Sent to PTO July 97

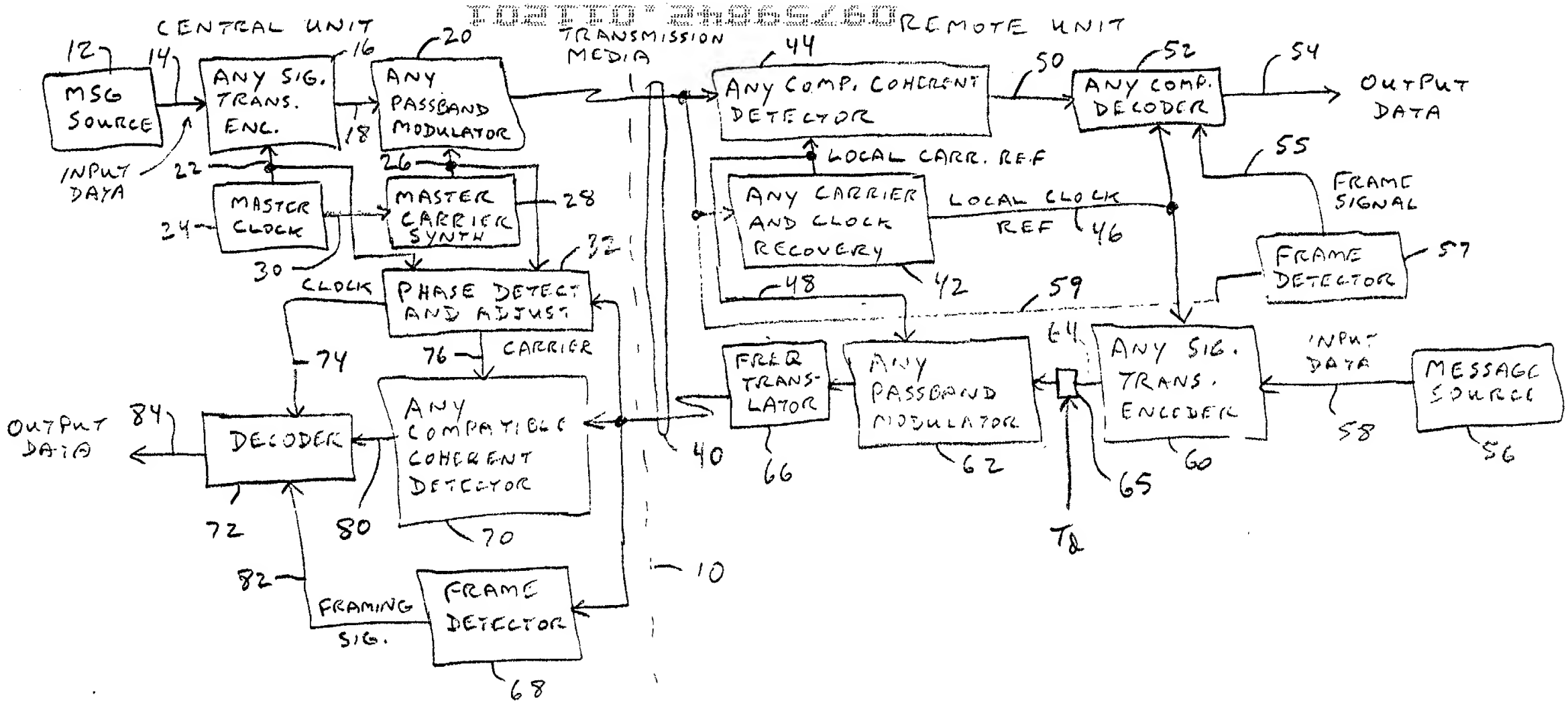


FIG. 1

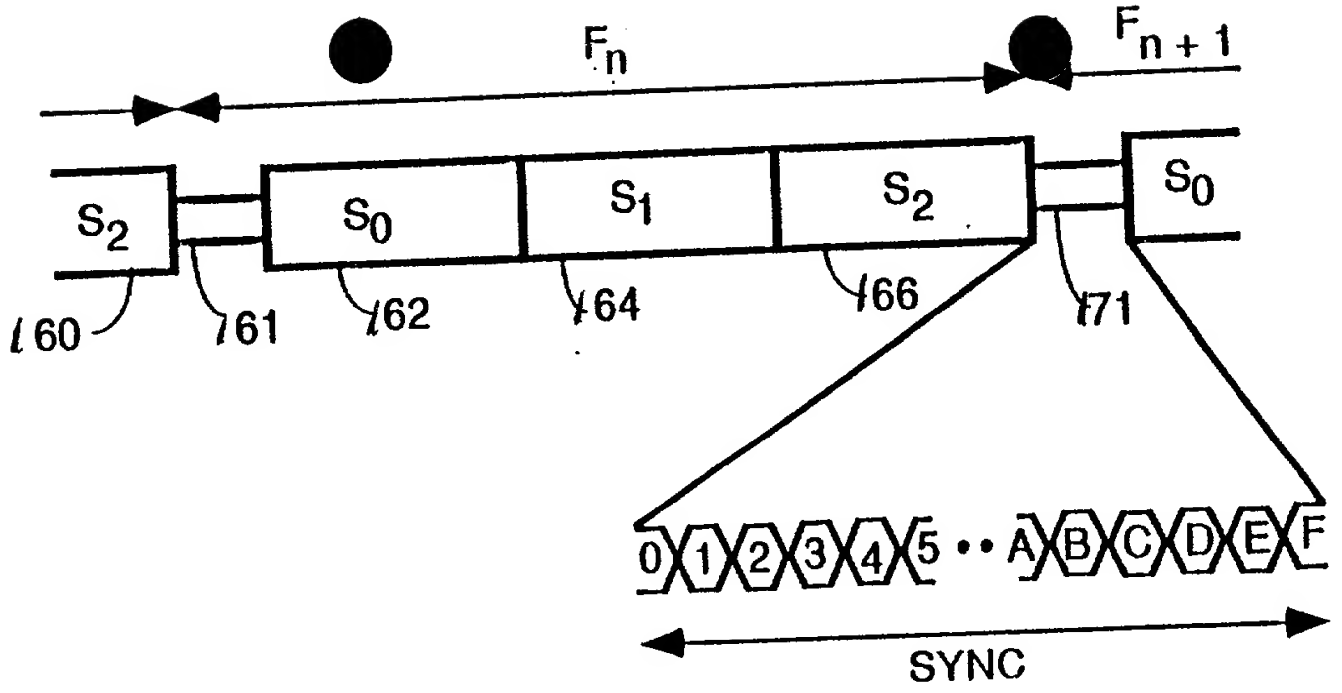

F_n
F_{n+1}
S_2
S_0
S_1
S_2
S_0
160
161
162
164
166
171
0 1 2 3 4 5 •• A B C D E F
SYNC

FIG. 4A

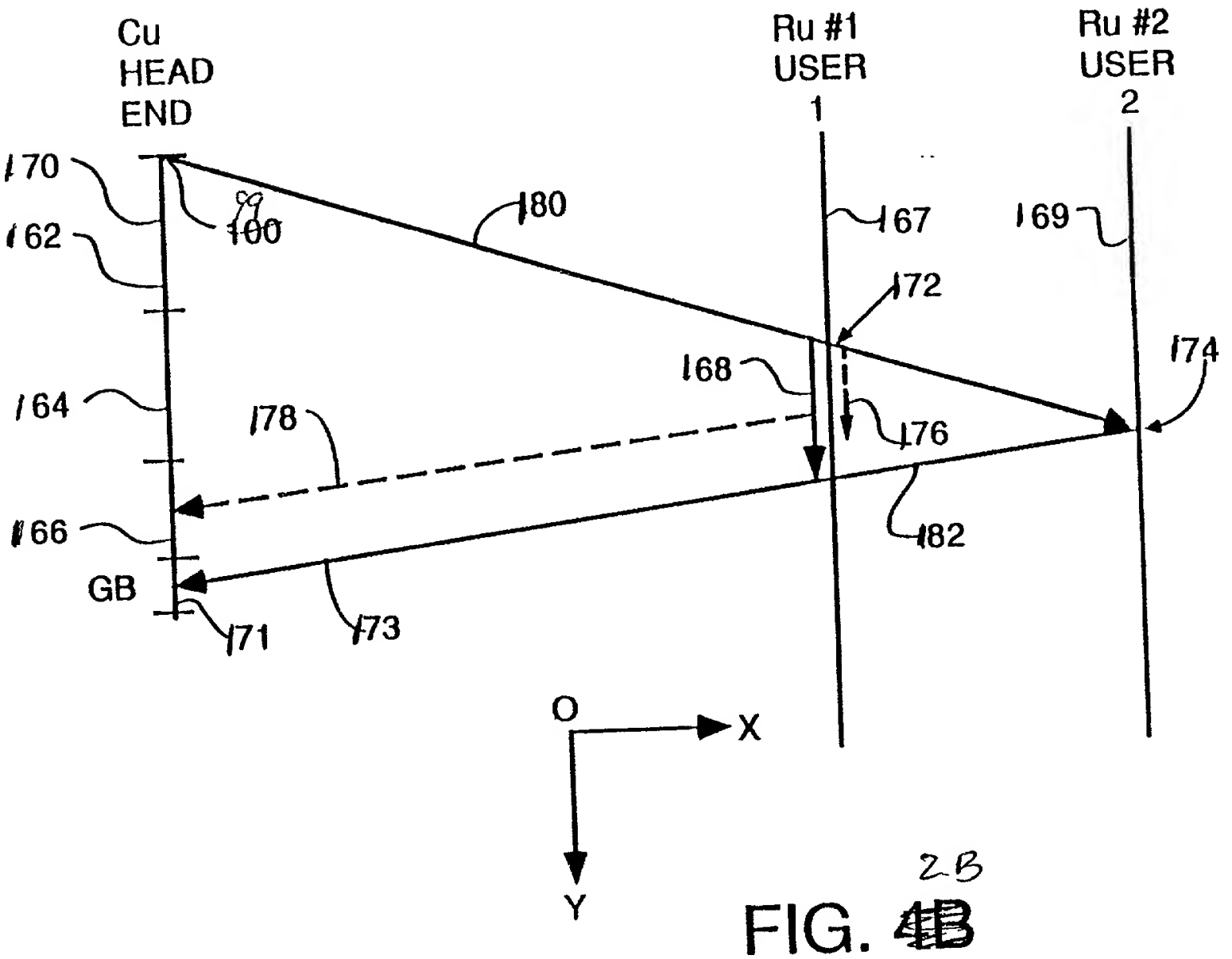

Cu
HEAD
END
Ru #1
USER
1
Ru #2
USER
2
170
162
164
166
GB
100
180
167
169
172
174
168
176
178
182
171
173
O
X
Y

FIG. 4B

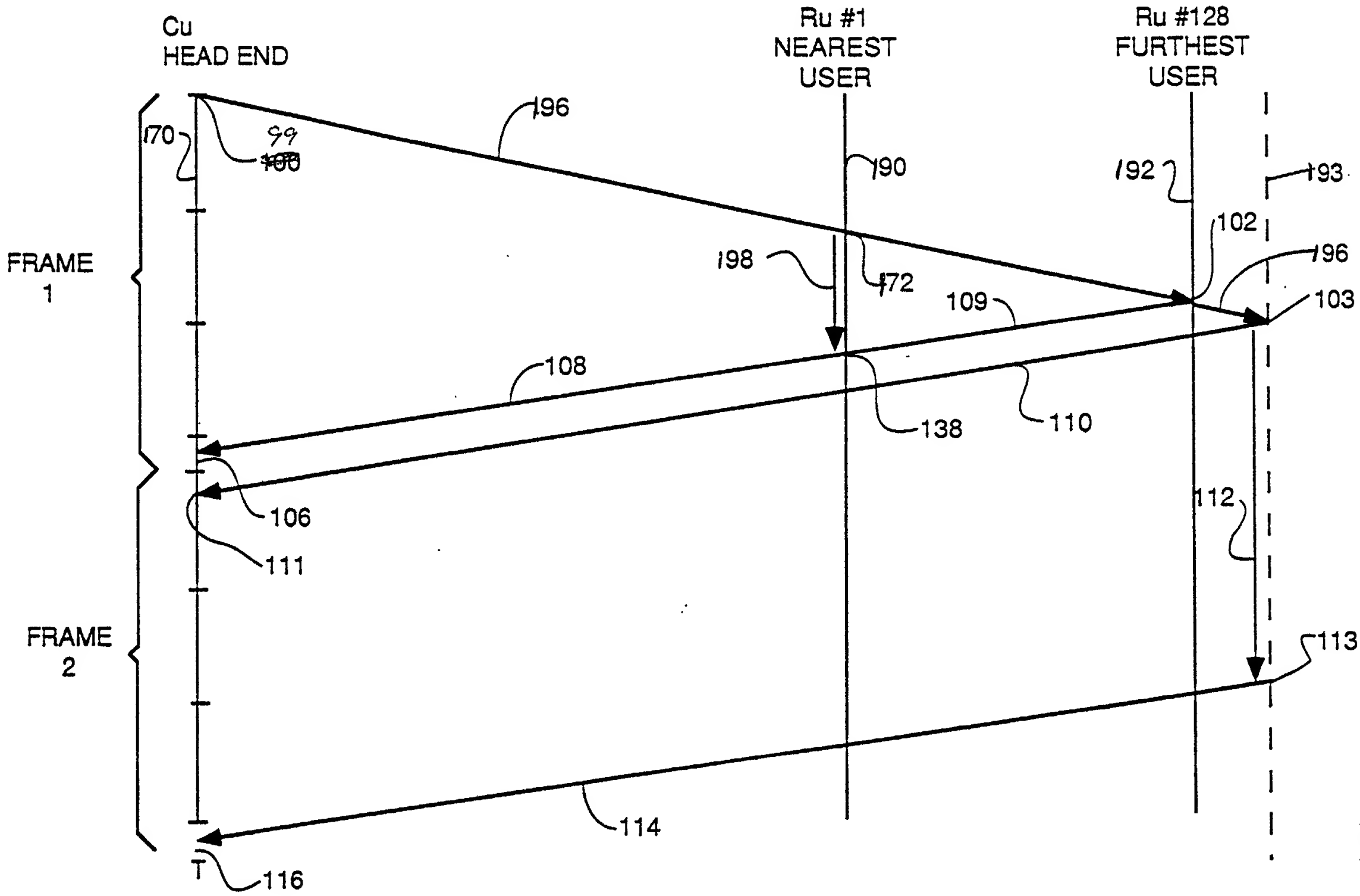

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
1
FRAME
2
T
170
99
100
196
190
192
193
102
198
172
109
103
108
138
110
106
111
112
113
114
116

FIG. 5

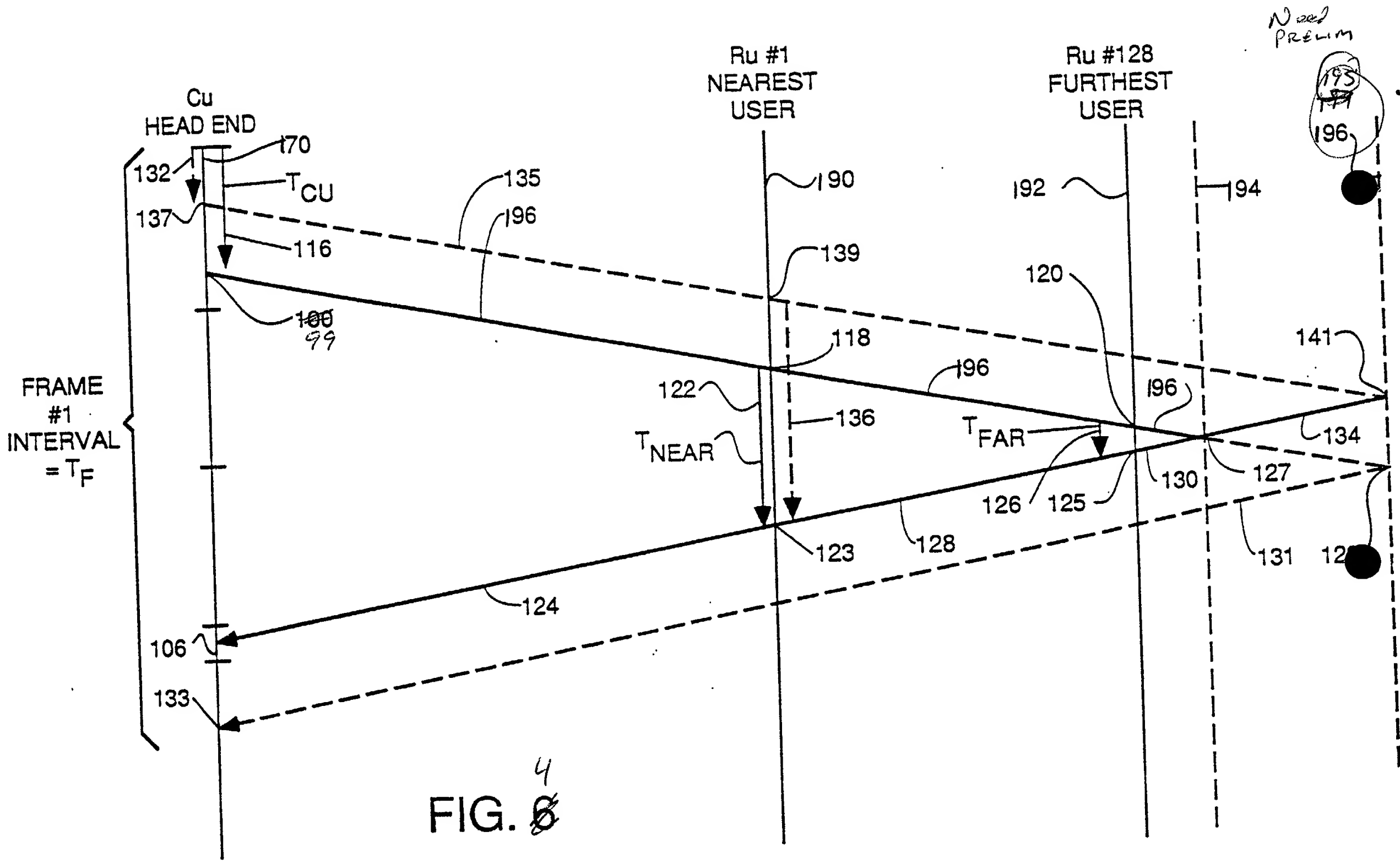

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
NEED PRELIM
195
196
170
132
T_{CU}
137
135
196
116
190
192
94
139
120
100
99
118
141
196
196
122
136
T_{FAR}
T_{NEAR}
134
130
127
126
125
123
128
131
124
106
133
FRAME
#1
INTERVAL
$= T_F$

FIG. 4

GENERAL RANGING PROCESS

FIG. ~~7A~~ 5A

CU WAITS FOR PREDETERMINED INTERVAL FROM START OF EACH FRAME AND THEN SENDS TRIGGER SIGNAL BARKER CODE TO RU'S DURING GAP

181
~~180~~

EACH RU TRYING TO SYNCHRONIZE RECEIVES BARKER CODE, SETS RECEIVE FRAME TIMING AND 1ST DELAY AND TRANSMITS SAME BARKER CODE TOWARD CU

183
~~182~~

CU MONITORS GAP FOR ACTIVITY BY PERFORMING CORRELATION BETWEEN ANY RECEIVED SIGNALS AND BARKER CODE

185
~~184~~

PEAK FOUND

CU B'CASTS A MESSAGE INDICATING IT FOUND ACTIVITY IN THE GAP

191
~~190~~

IN RESPONSE, EACH RU TRYING TO SYNCHRONIZE SENDS ITS UNIQUE SIGNATURE TOWARD THE CU

193
~~192~~

TO FIG. ~~7B~~ 5B

NO PEAK

CU B'CASTS A MESSAGE TO ALL RU'S TELLING THEM TO ADJUST THEIR DELAYS AND TRY AGAIN

186

EACH RU TRYING TO SYNCHRONIZE INCREMENTS ITS DELAY AND RETRANSMITS THE BARKER CODE

188

FROM FIG. 4A

CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.

CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.

GREATER THAN 50% ACTIVITY

CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.

204

EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.

206

RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION

208

TO FIG. 5C

50% ACTIVITY DETECTED

CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.

RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.

200

CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.

202

FIG. 5B

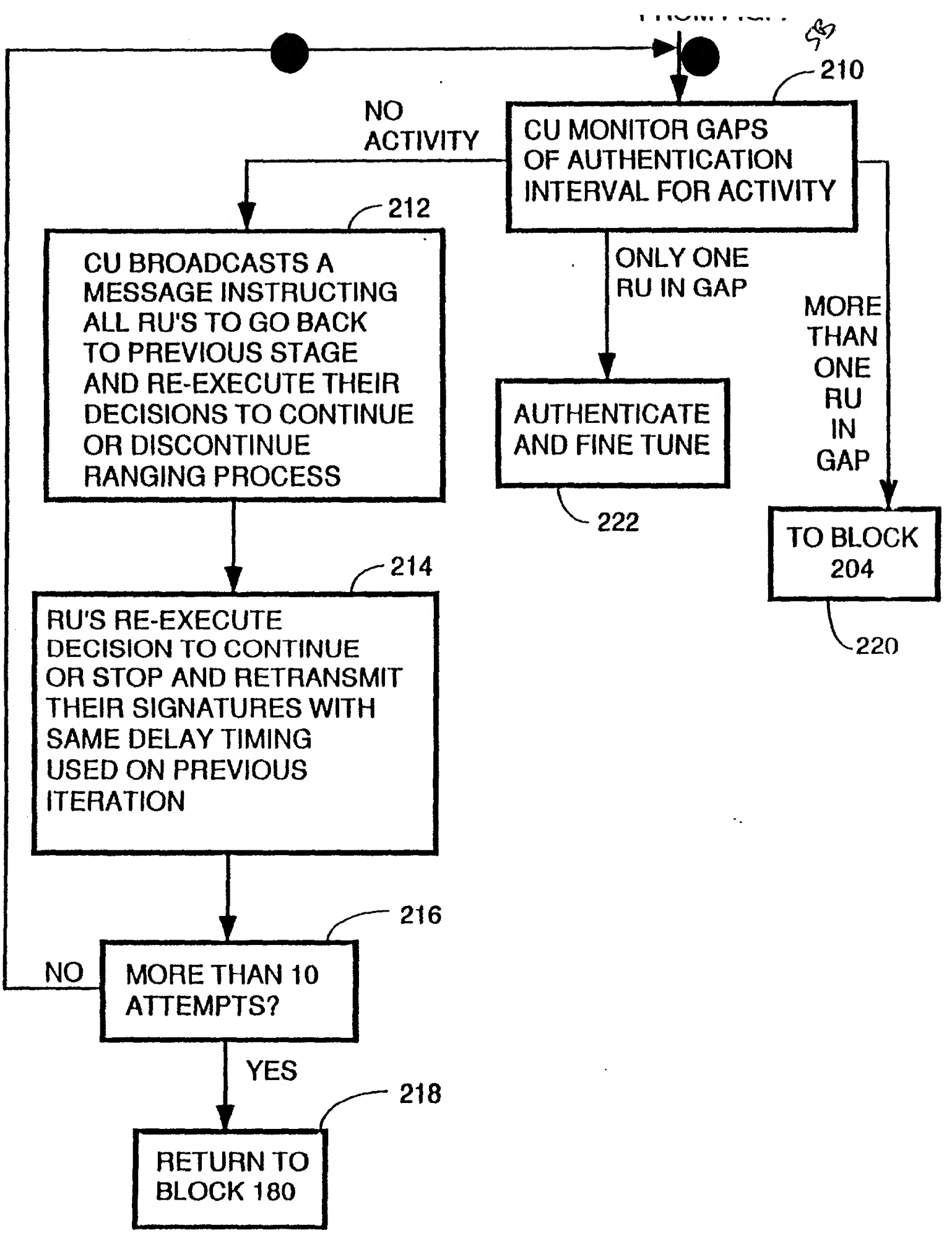
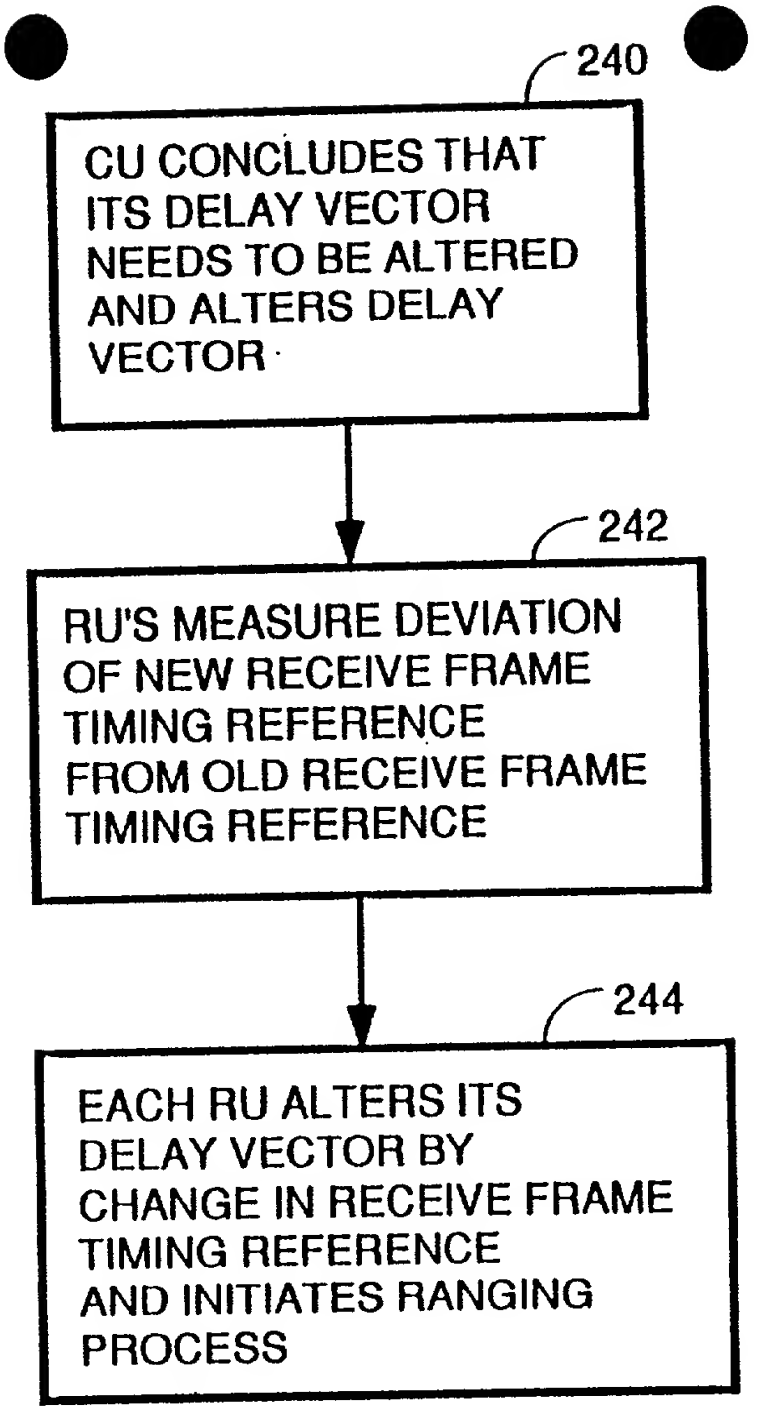

210
NO ACTIVITY
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
MORE THAN ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C ~~7C~~



6

FIG. 8

DEAD RECKONING RE-SYNC

CU CONCLUDES IT MUST ALTER ITS DELAY VECTOR TO ALLOW THE FARTHEST RU'S TO SYNCHRONIZE TO THE SAME FRAME AS THE NEAREST RU'S AND BROADCASTS A MESSAGE TO ALL RU'S INDICATING WHEN AND BY HOW MUCH IT WILL ALTER ITS DELAY VECTOR

248

EACH RU RECEIVES BROADCAST AND ALTERS ITS DELAY VECTOR BY AMOUNT INSTRUCTED AT TIME CU ALTERS ITS DELAY VECTOR

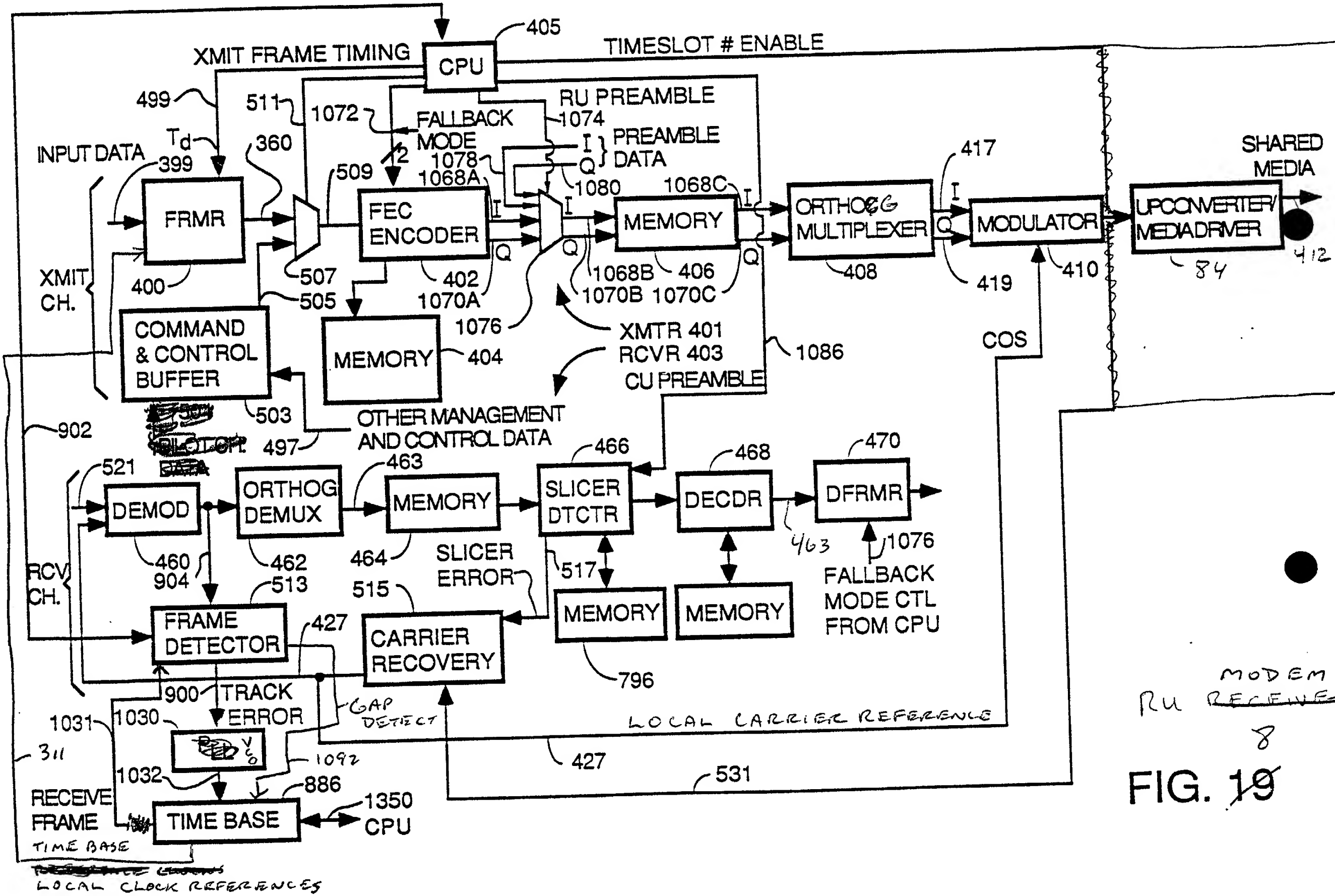
250

EACH RU REINITIATES SYNCHRONIZATION PROCESS

FIG. 7

PRECURSOR EMBODIMENT

RU DIGITAL MODEM BLOCK DIAGRAM



MODEM RU RECEIVE 8

FIG. 19

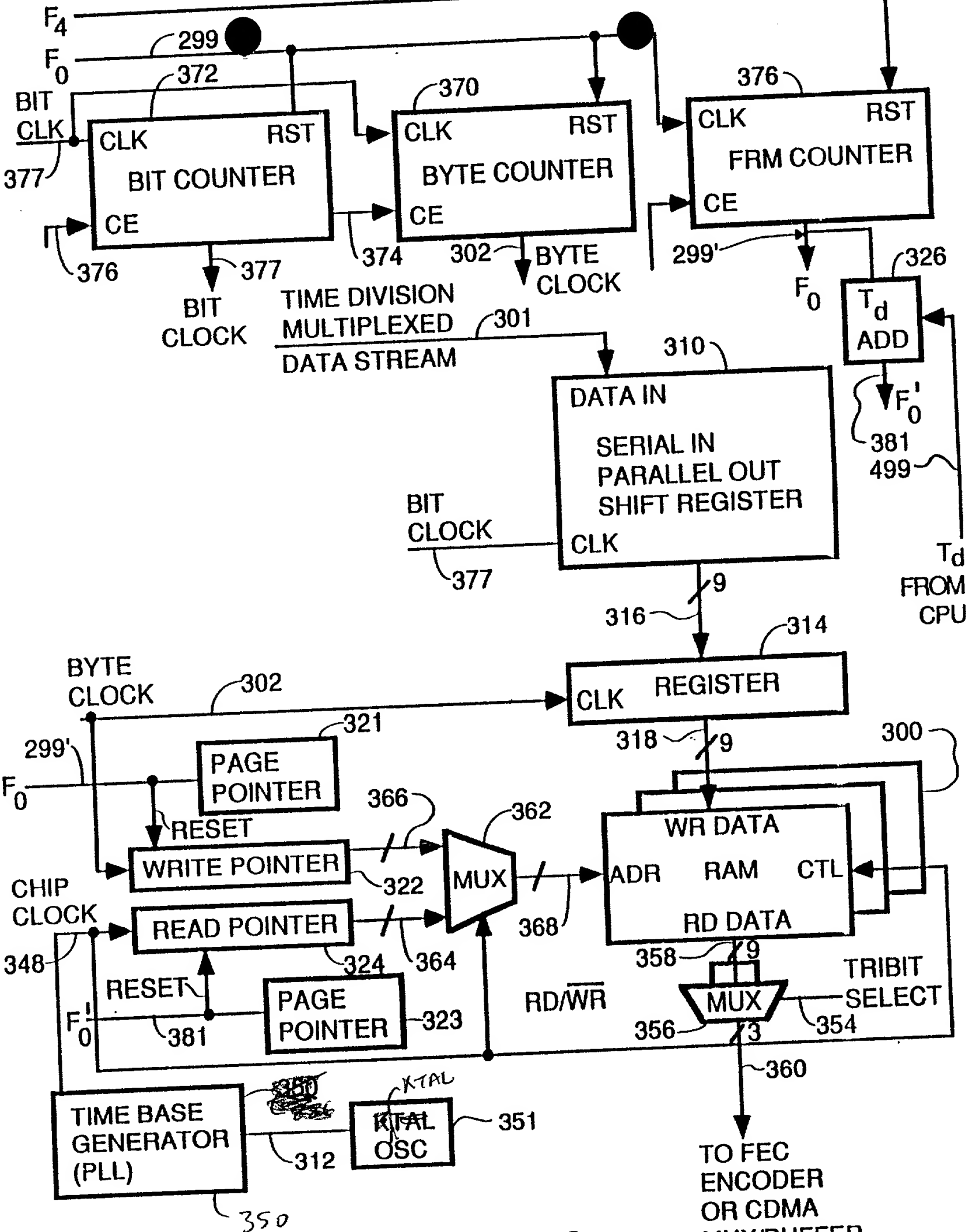

F4
F0
299
372
370
376
BIT CLK
CLK
RST
BIT COUNTER
CE
377
BYTE COUNTER
FRM COUNTER
376
374
302
BYTE CLOCK
299'
326
BIT CLOCK
377
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
Td ADD
F'0
381
499
BIT CLOCK
Td FROM CPU
9
316
314
REGISTER
BYTE CLOCK
302
321
300
318
299'
PAGE POINTER
366
362
RESET
WRITE POINTER
322
MUX
WR DATA
ADR
RAM
CTL
RD DATA
CHIP CLOCK
READ POINTER
368
348
324
364
358
TRIBIT SELECT
RESET
RD/WR
356
354
360
TIME BASE GENERATOR (PLL)
XTAL
OSC
351
312
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 12

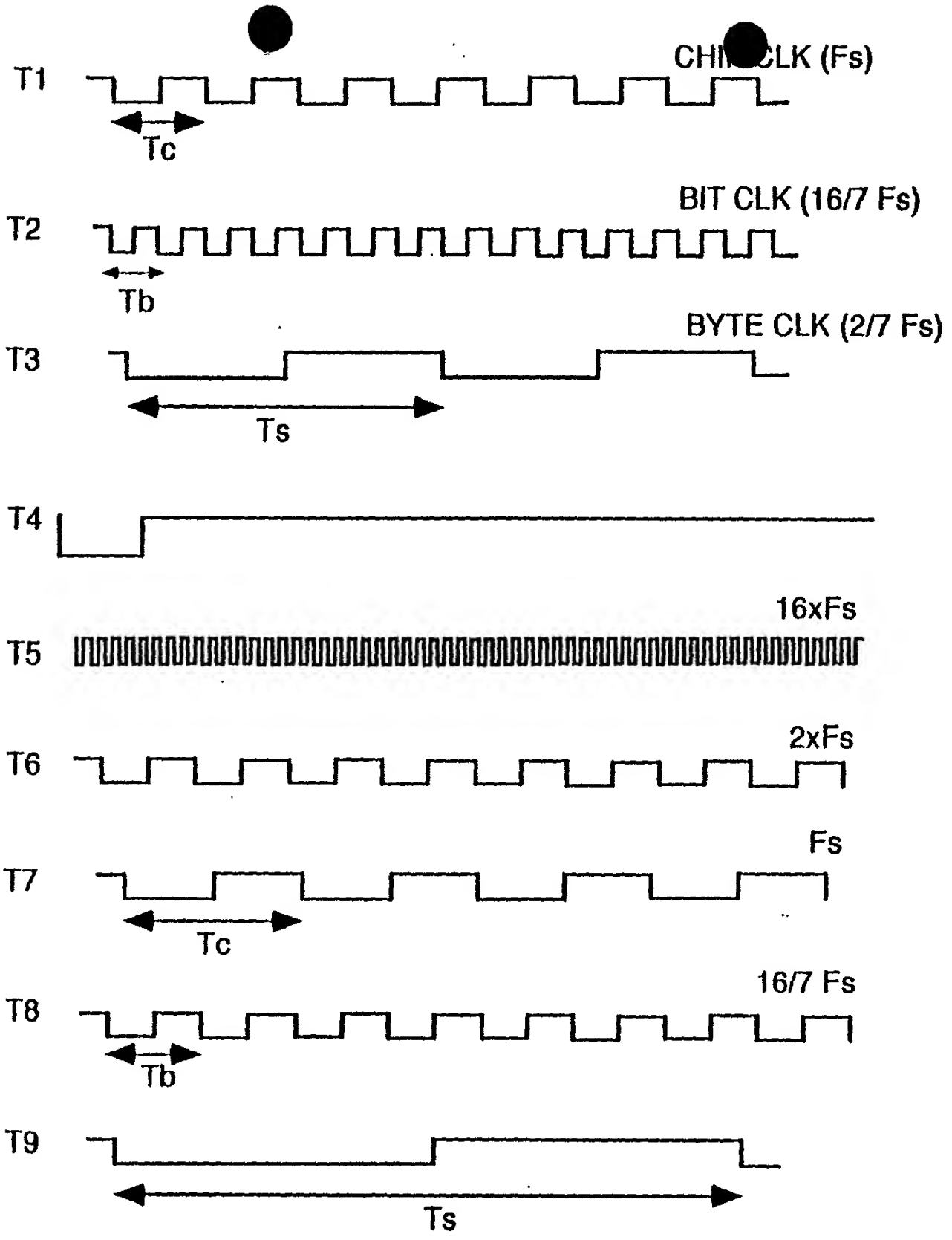
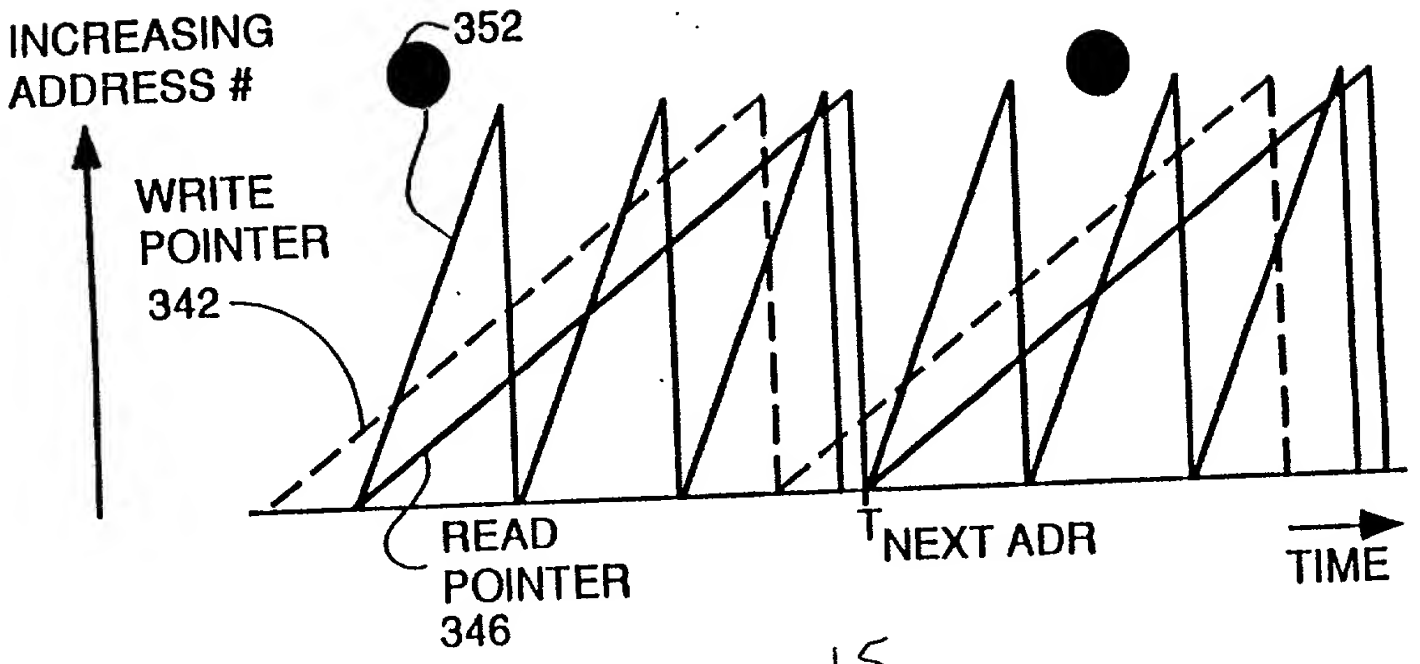
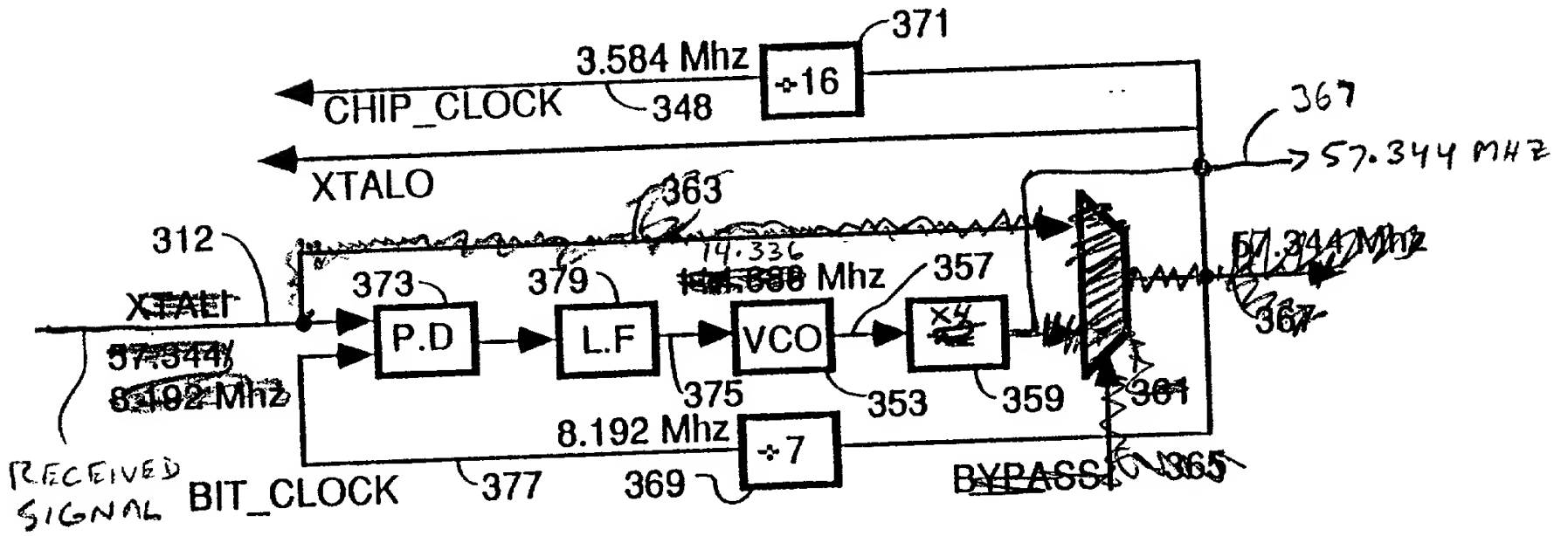


FIG. 13



15

FIG. 17



11

FIG. 18

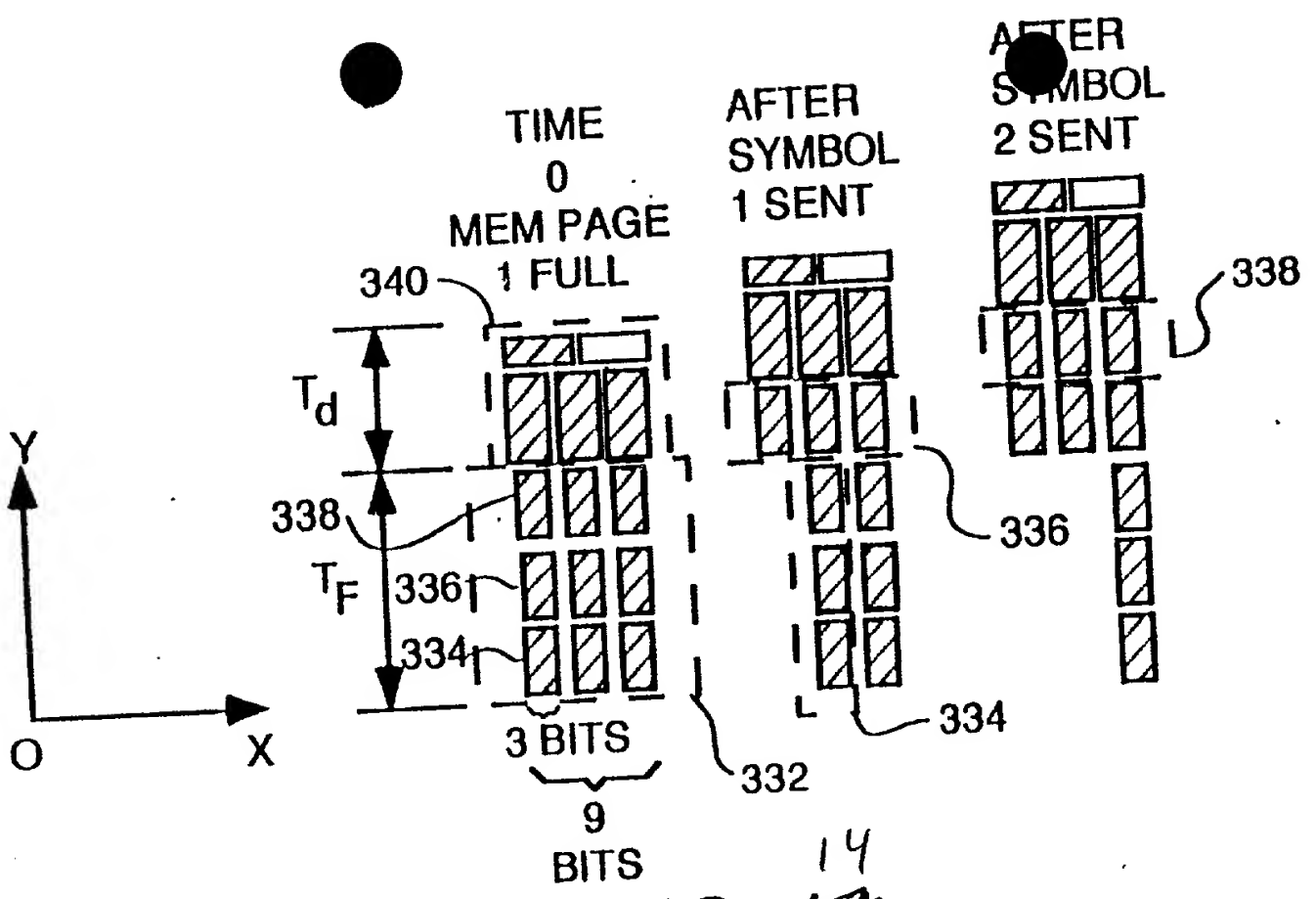


FIG. 14

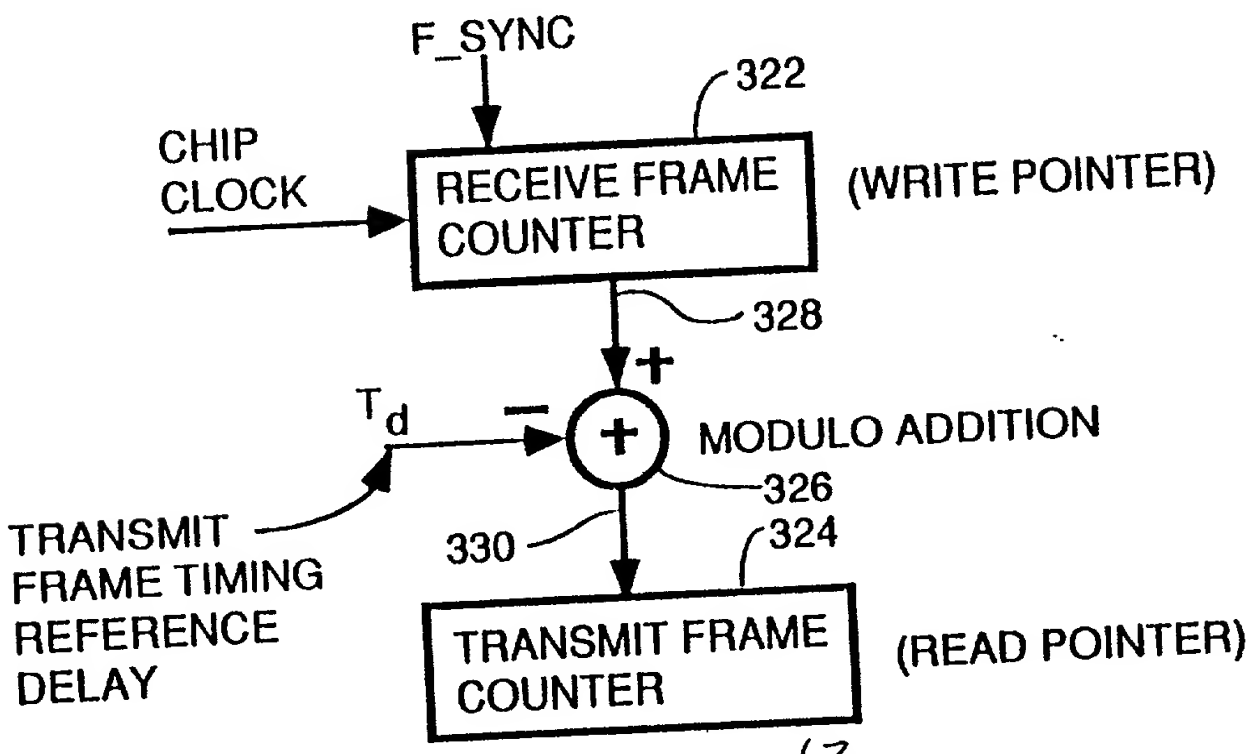


FIG. 12

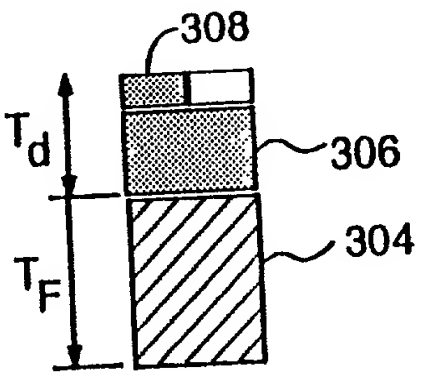


FIG. 13

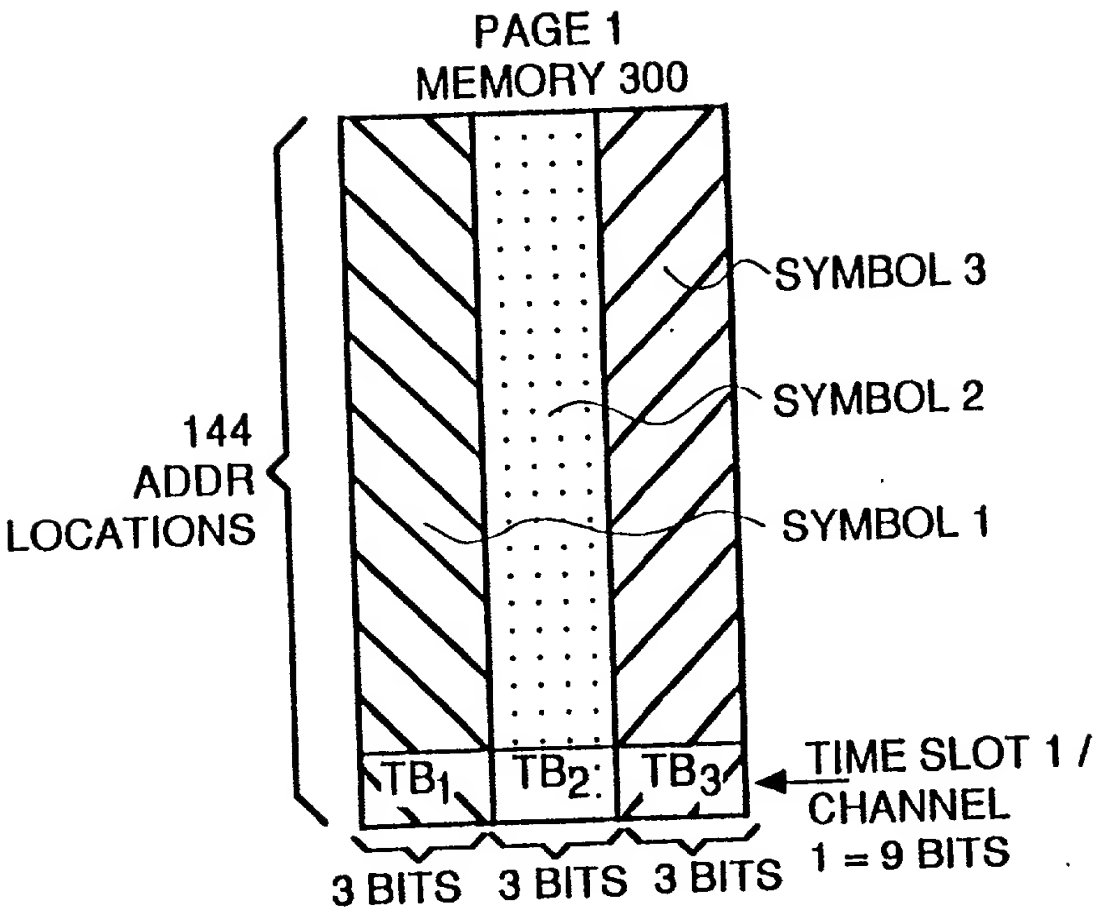
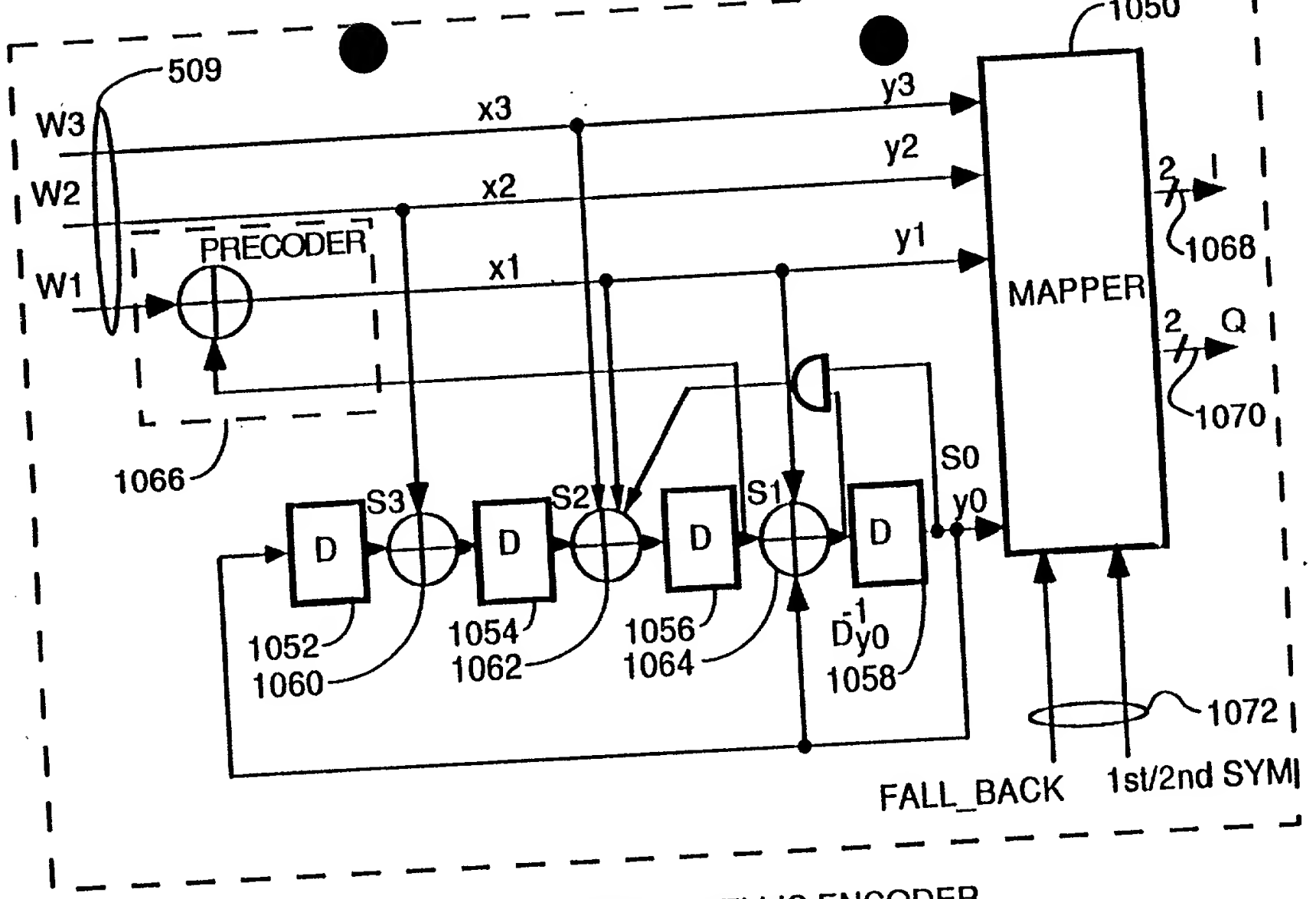

PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. 20

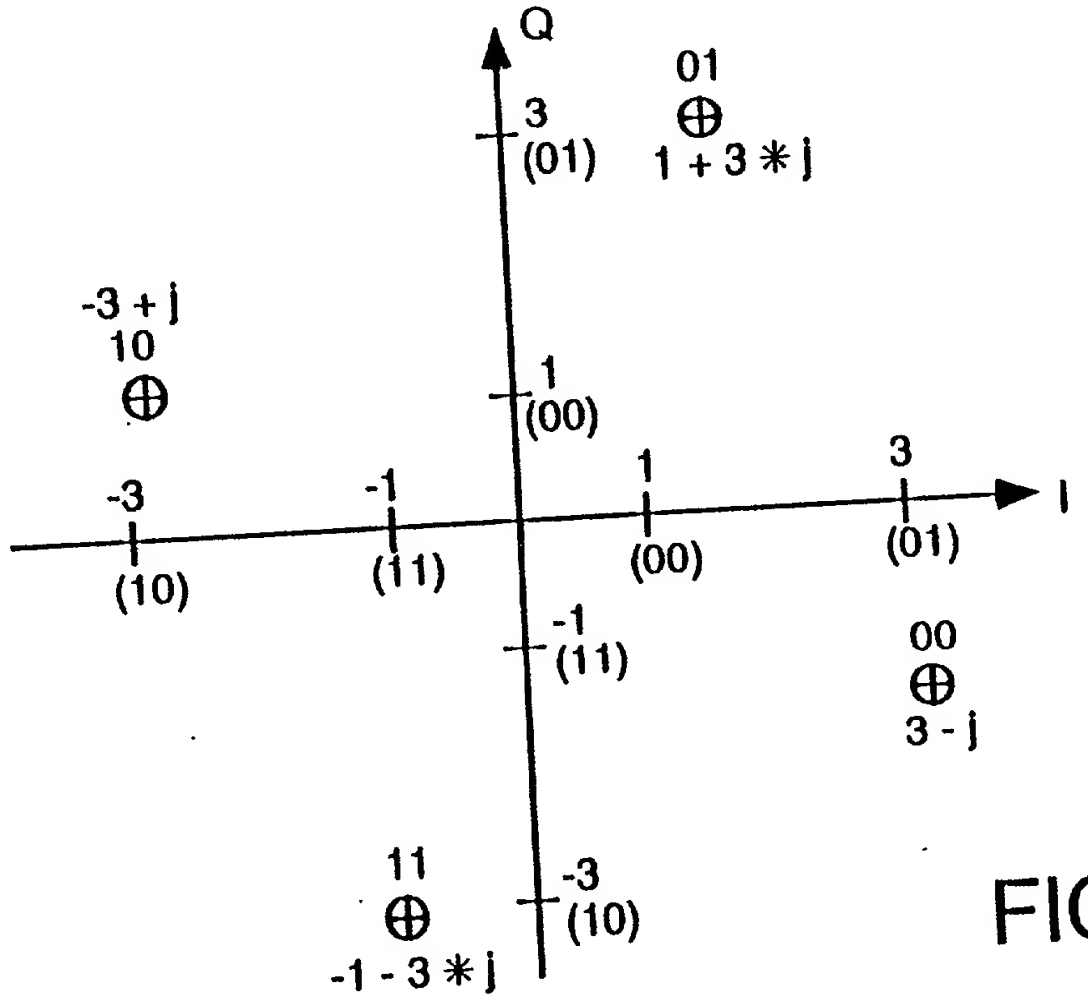


PREFERRED TRELLIS ENCODER

FIG. 42

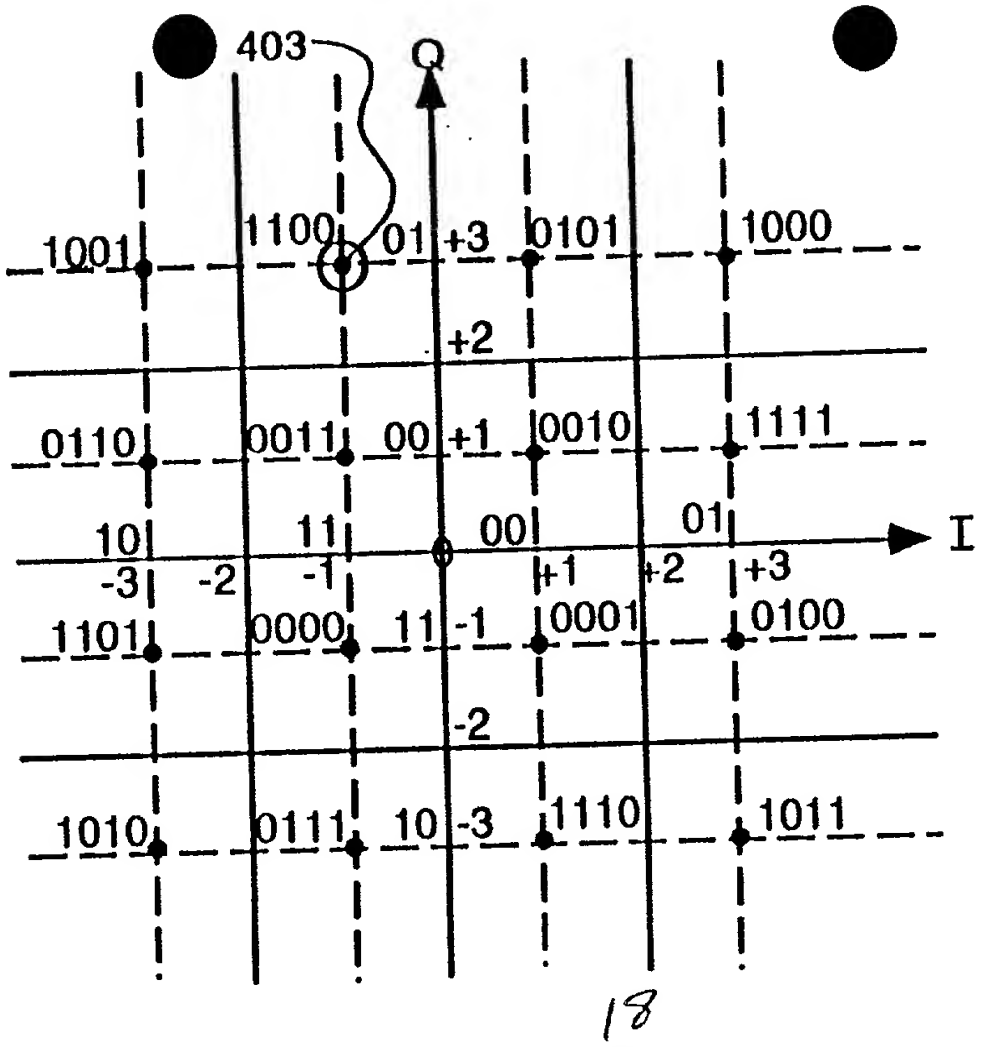
17

MAPPING FOR FALL-BACK MODE - LSB'S



21

FIG. 43



18

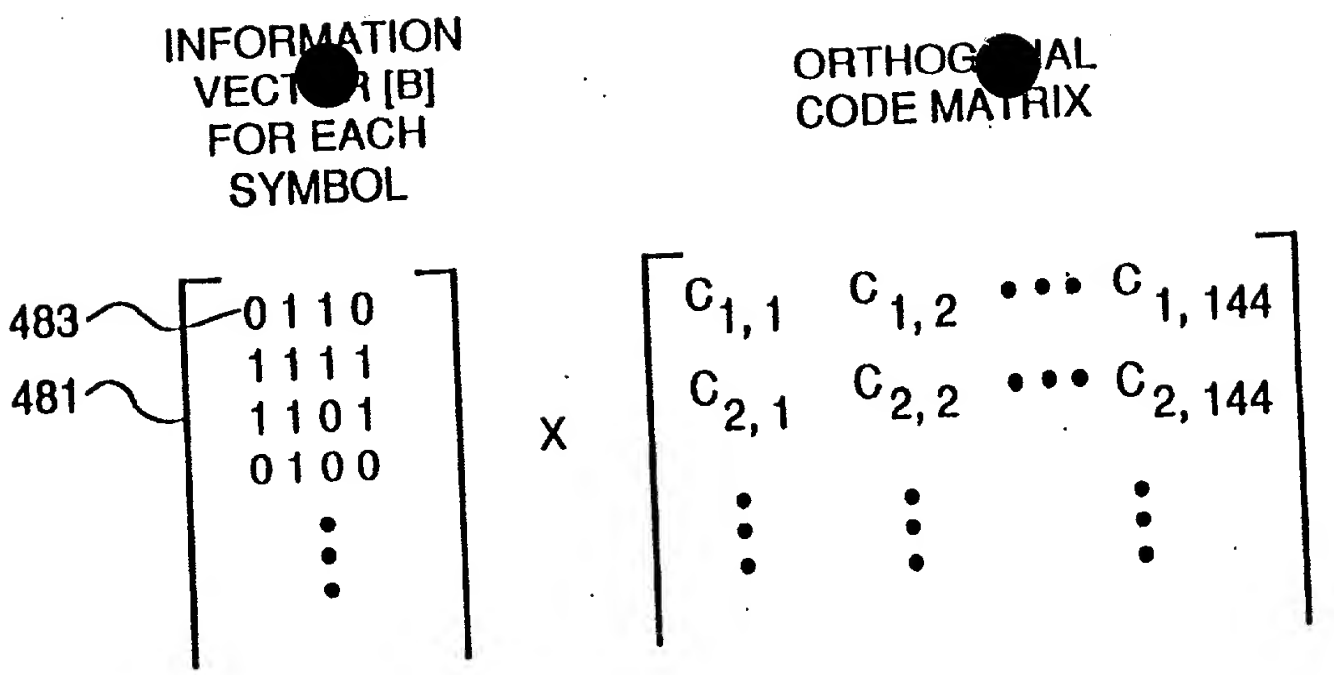
FIG. 21

CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 - j
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3*j
1001	101	011	= -3 + 3*j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
1100	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

403

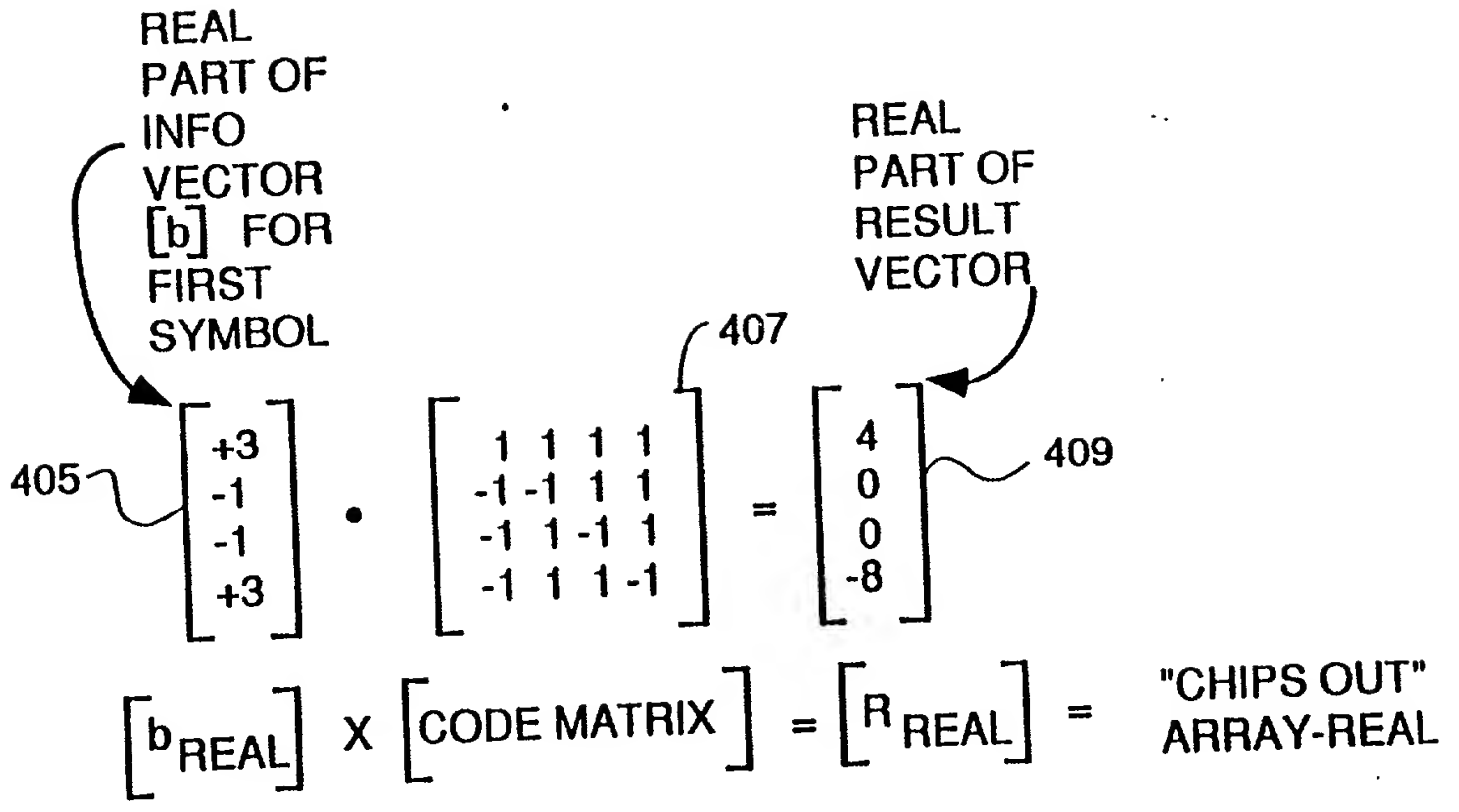
19

FIG. 22



20A

FIG. ~~23~~A



20B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

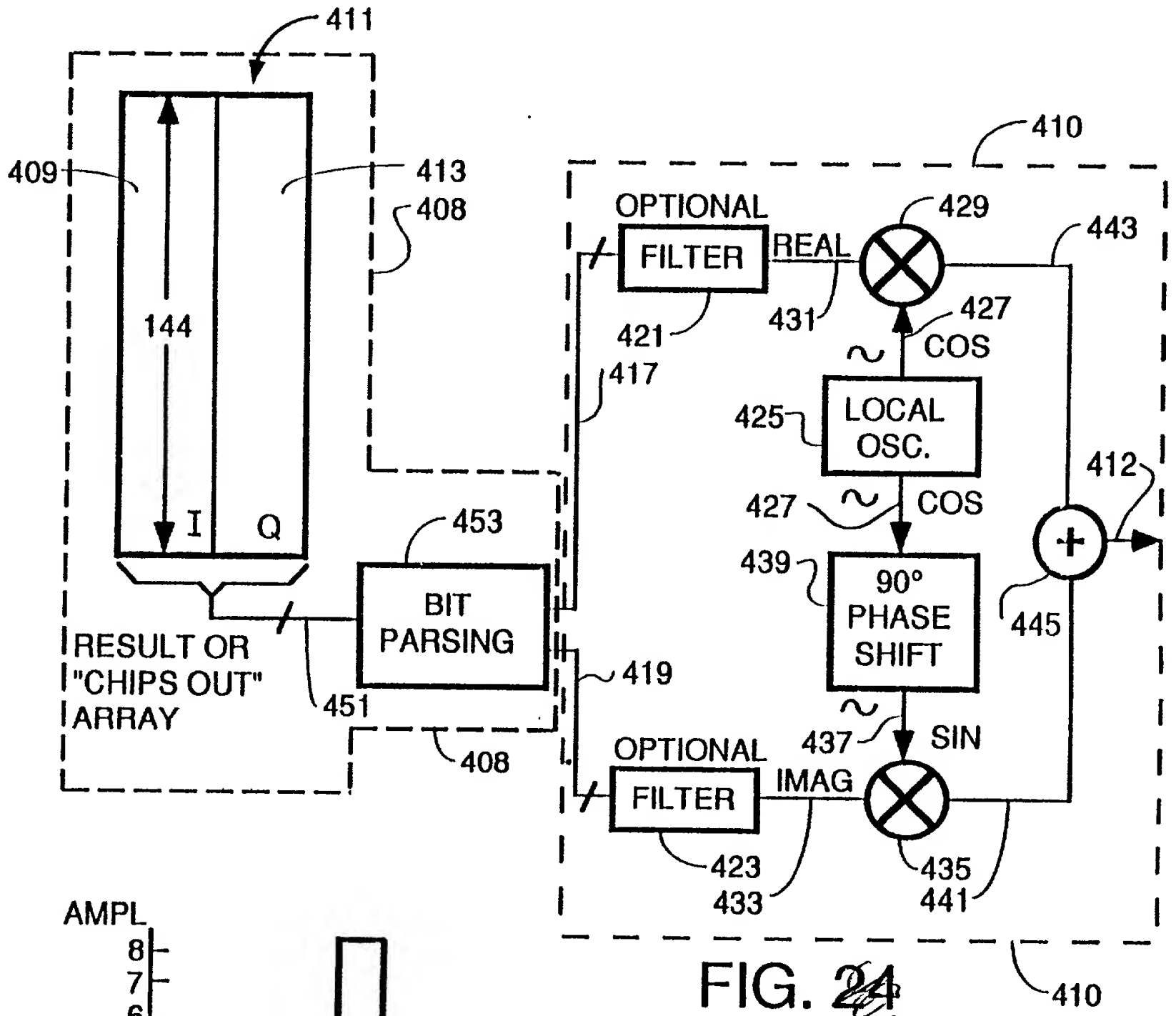

411
409
413
408
144
I
Q
453
BIT PARSING
RESULT OR "CHIPS OUT" ARRAY
451
419
408
410
OPTIONAL
FILTER
REAL
429
443
421
431
427
COS
417
425
LOCAL OSC.
412
427
COS
439
90° PHASE SHIFT
445
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 24

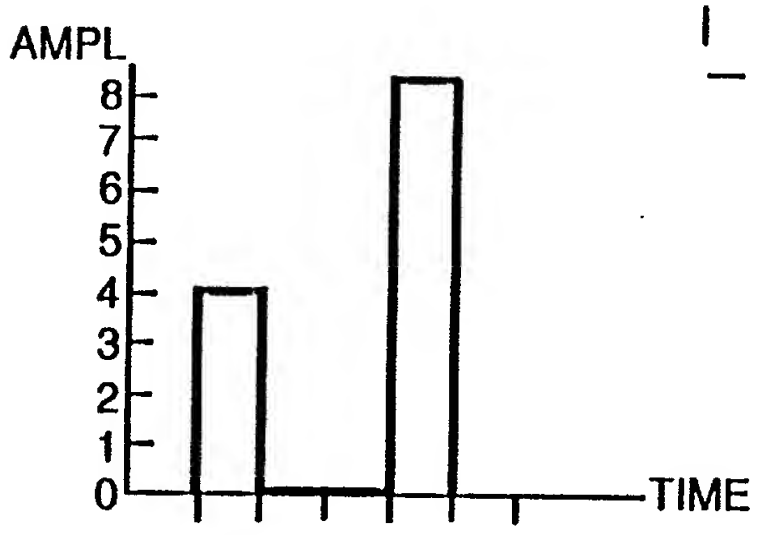
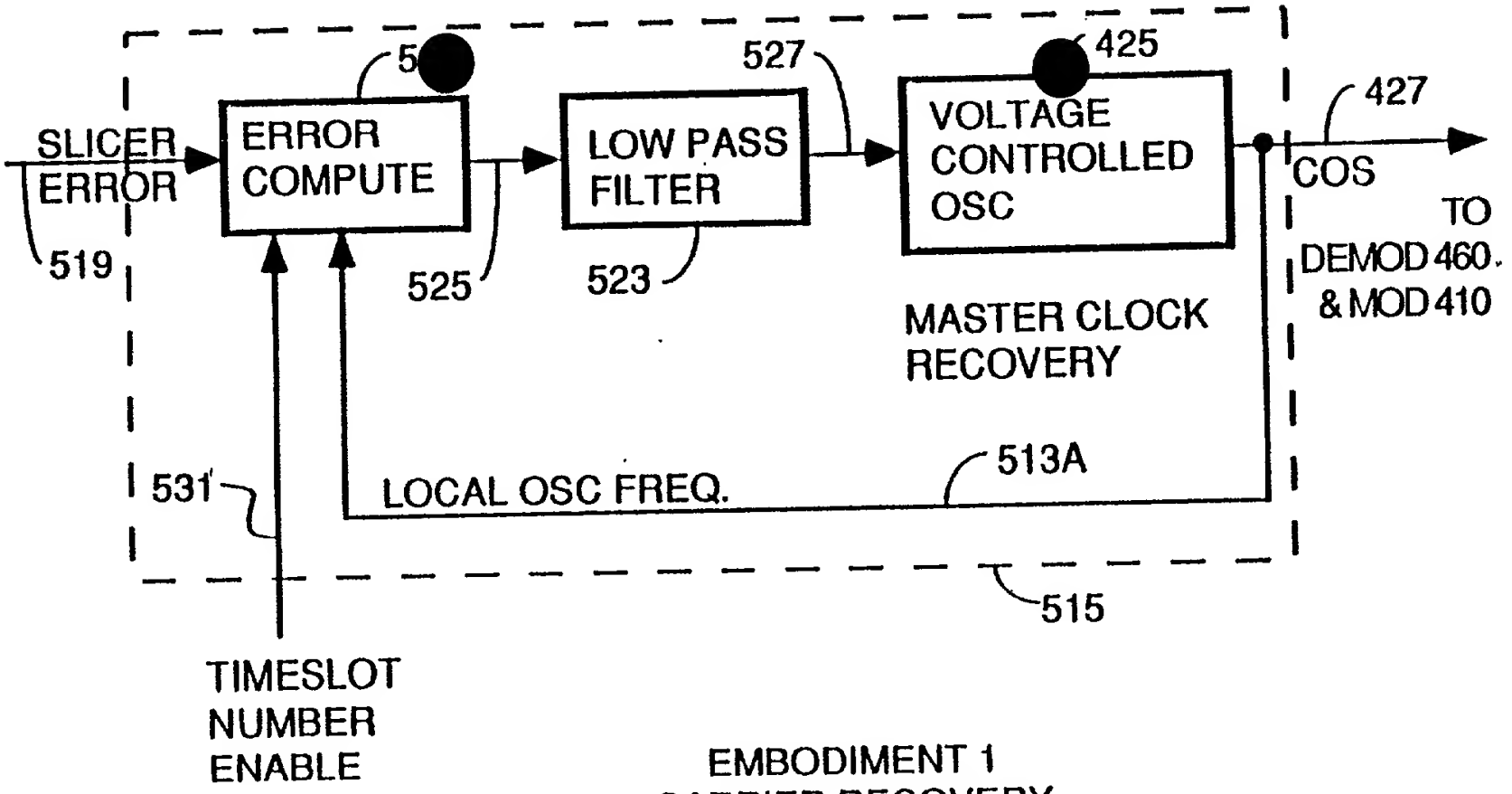

AMPL
8
7
6
5
4
3
2
1
0
TIME

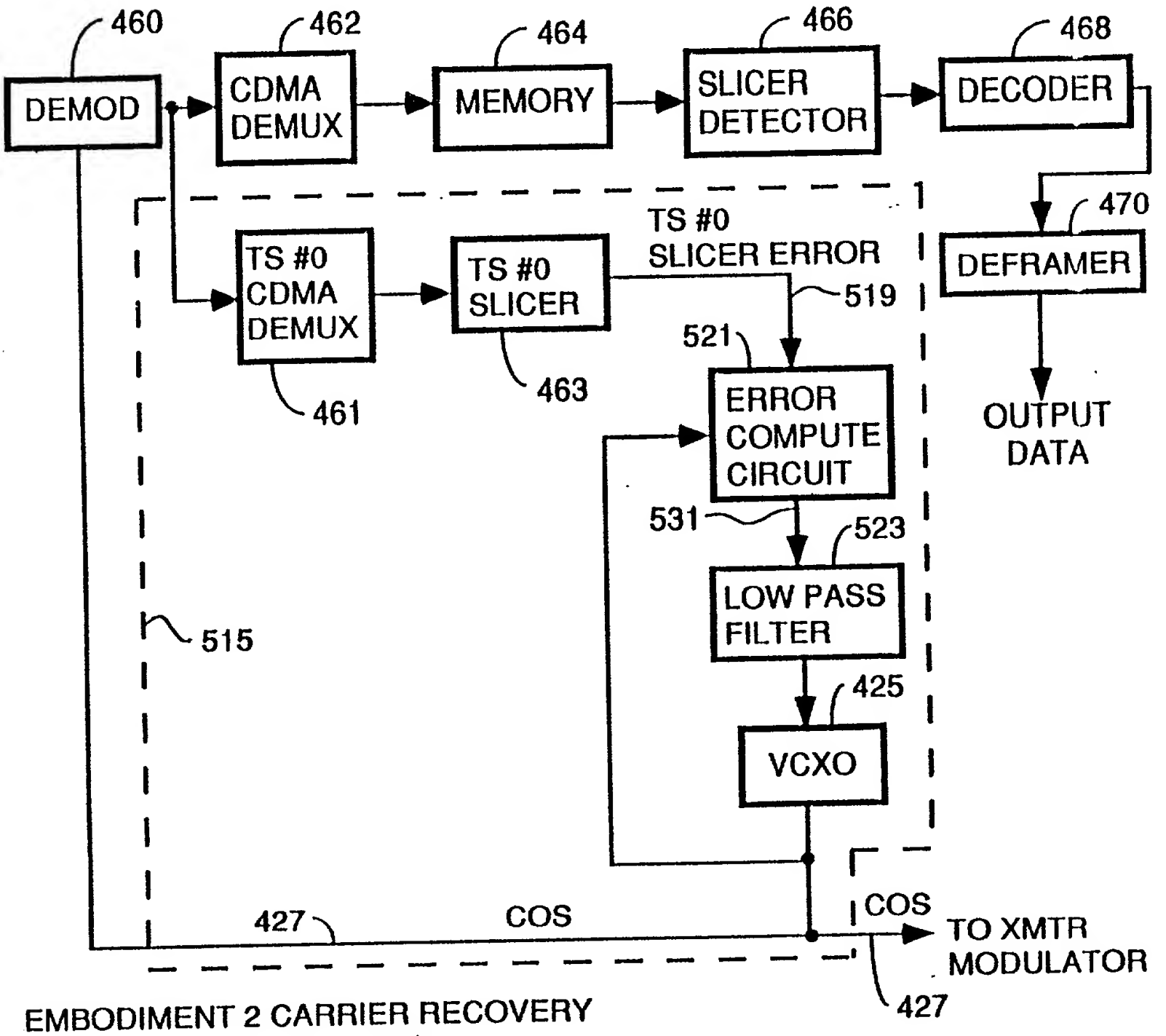
FIG. 25



EMBODIMENT 1
CARRIER RECOVERY

FIG. 35

25



EMBODIMENT 2 CARRIER RECOVERY

FIG. 36

26

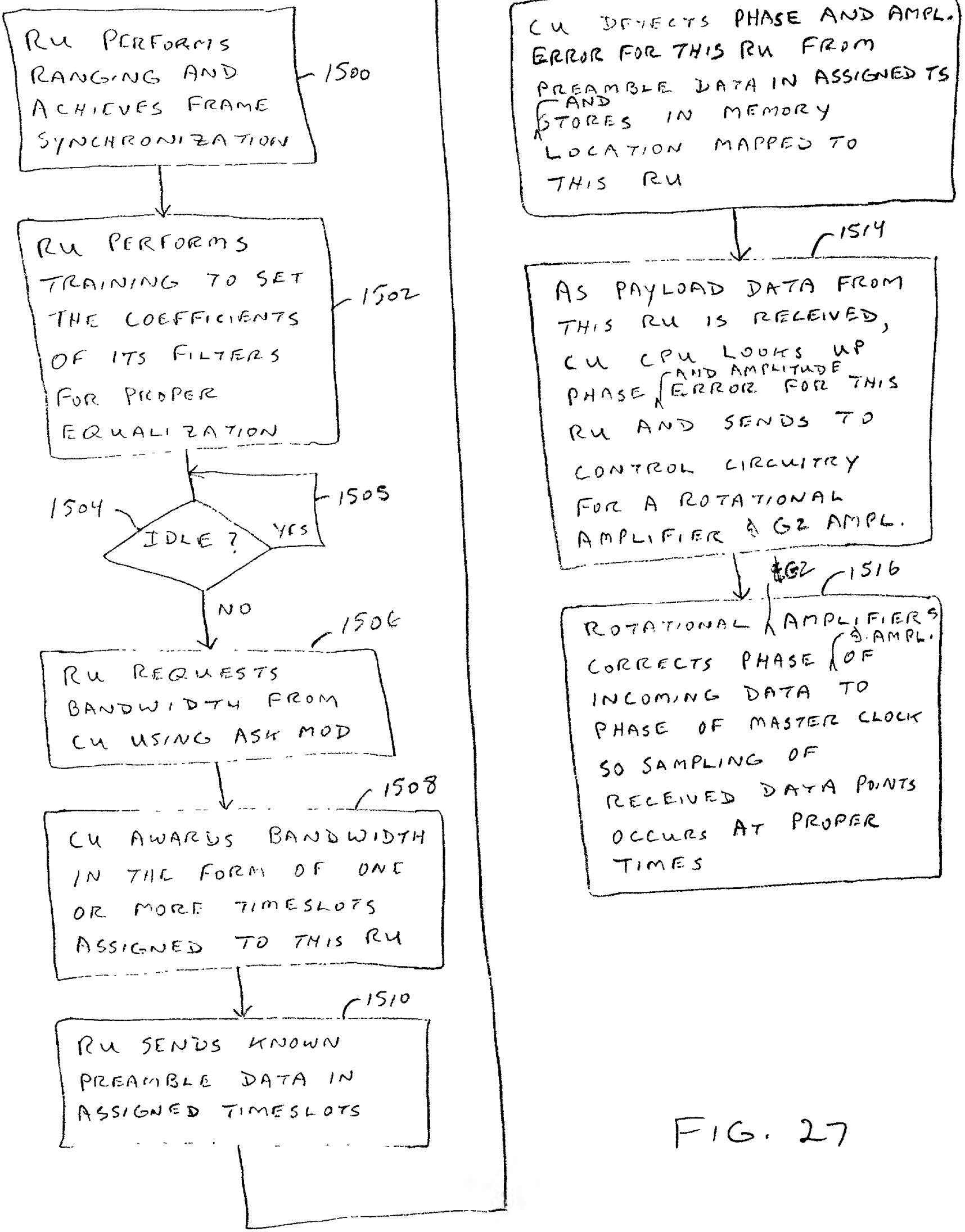
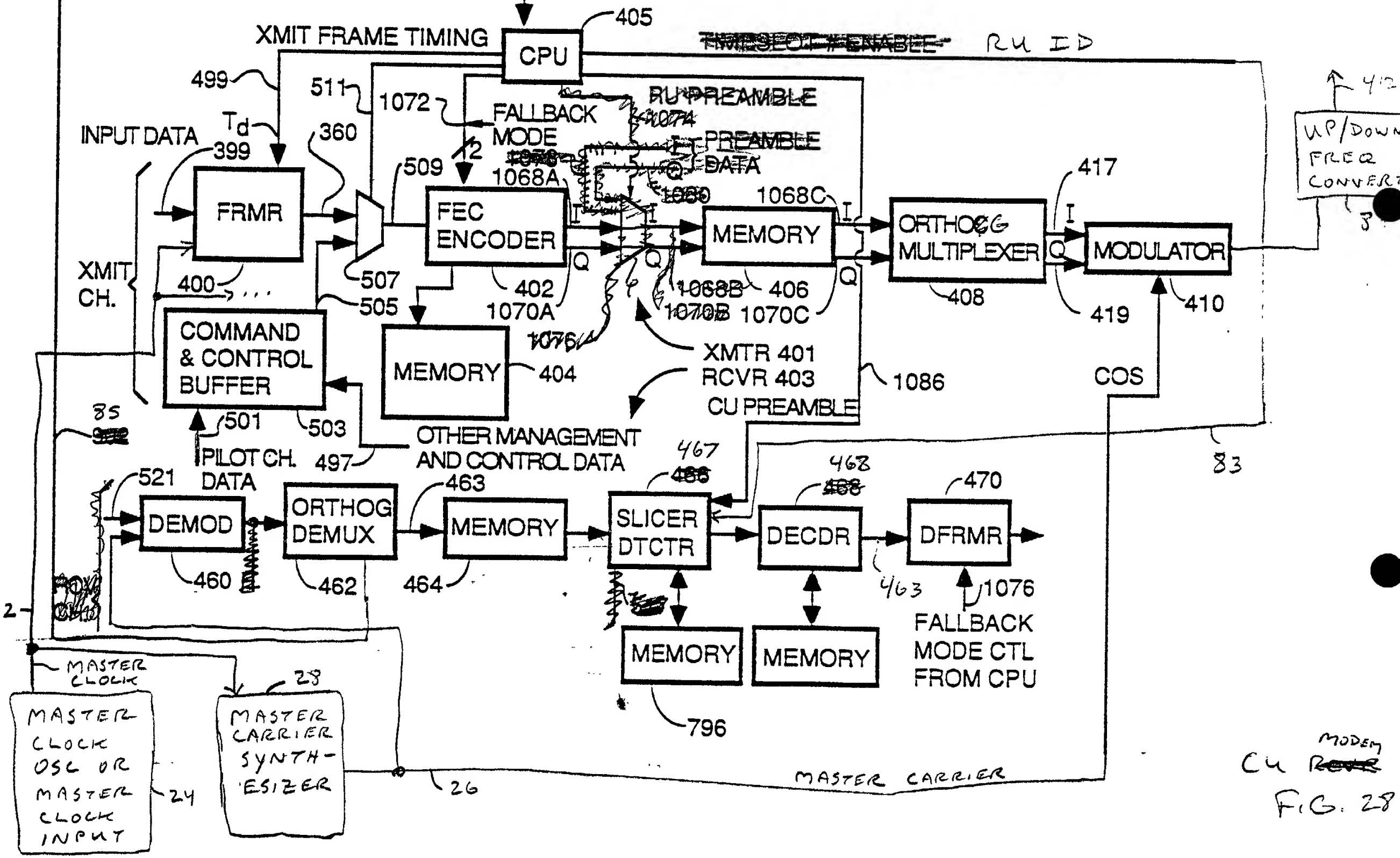

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
1506
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1508
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1510
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1512
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1514
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1516
ROTATIONAL AMPLIFIERS & G2 AMPL. CORRECTS PHASE OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES

FIG. 27

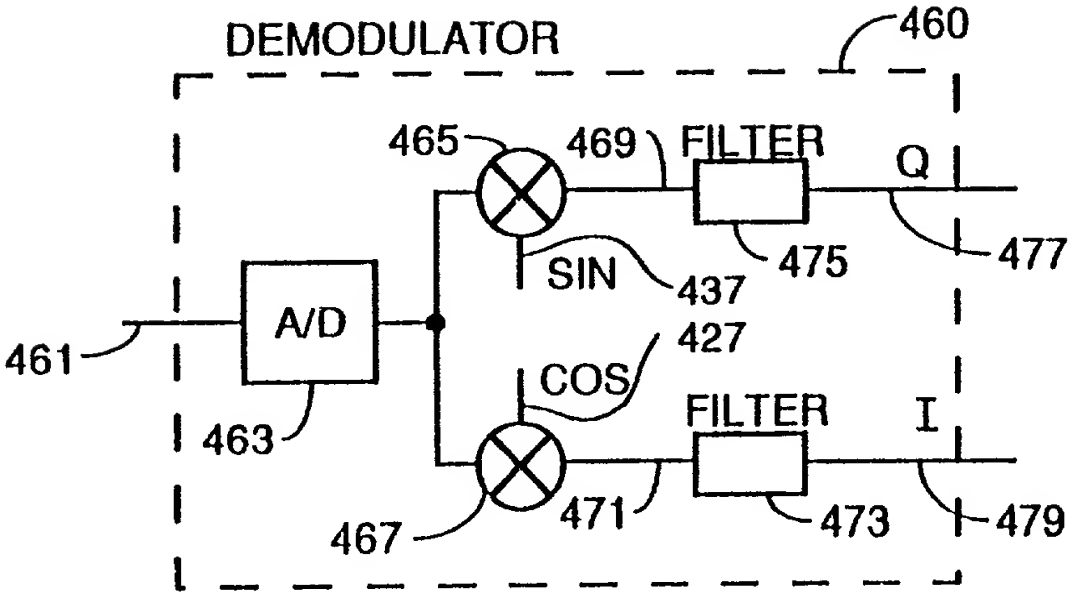
CU

DIGITAL MODEM BLOCK DIAGRAM



CU MODEM

FIG. 28


DEMODULATOR
460
465
469
FILTER
Q
475
477
SIN
437
A/D
461
427
COS
FILTER
I
463
467
471
473
479

29

FIG. 26

Page 94, Line 80" 2+965,760
Removed to 793

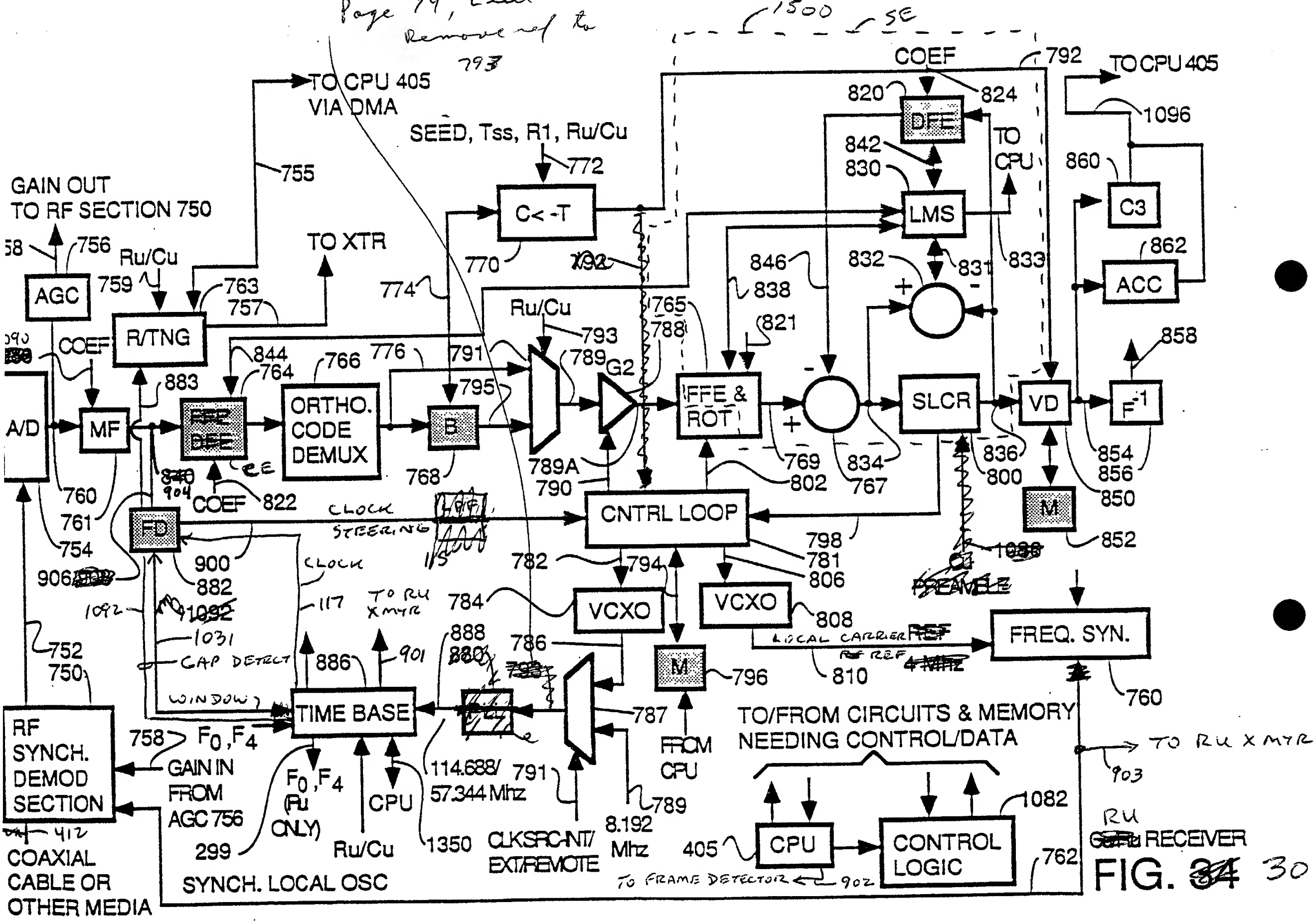


FIG. 84 30

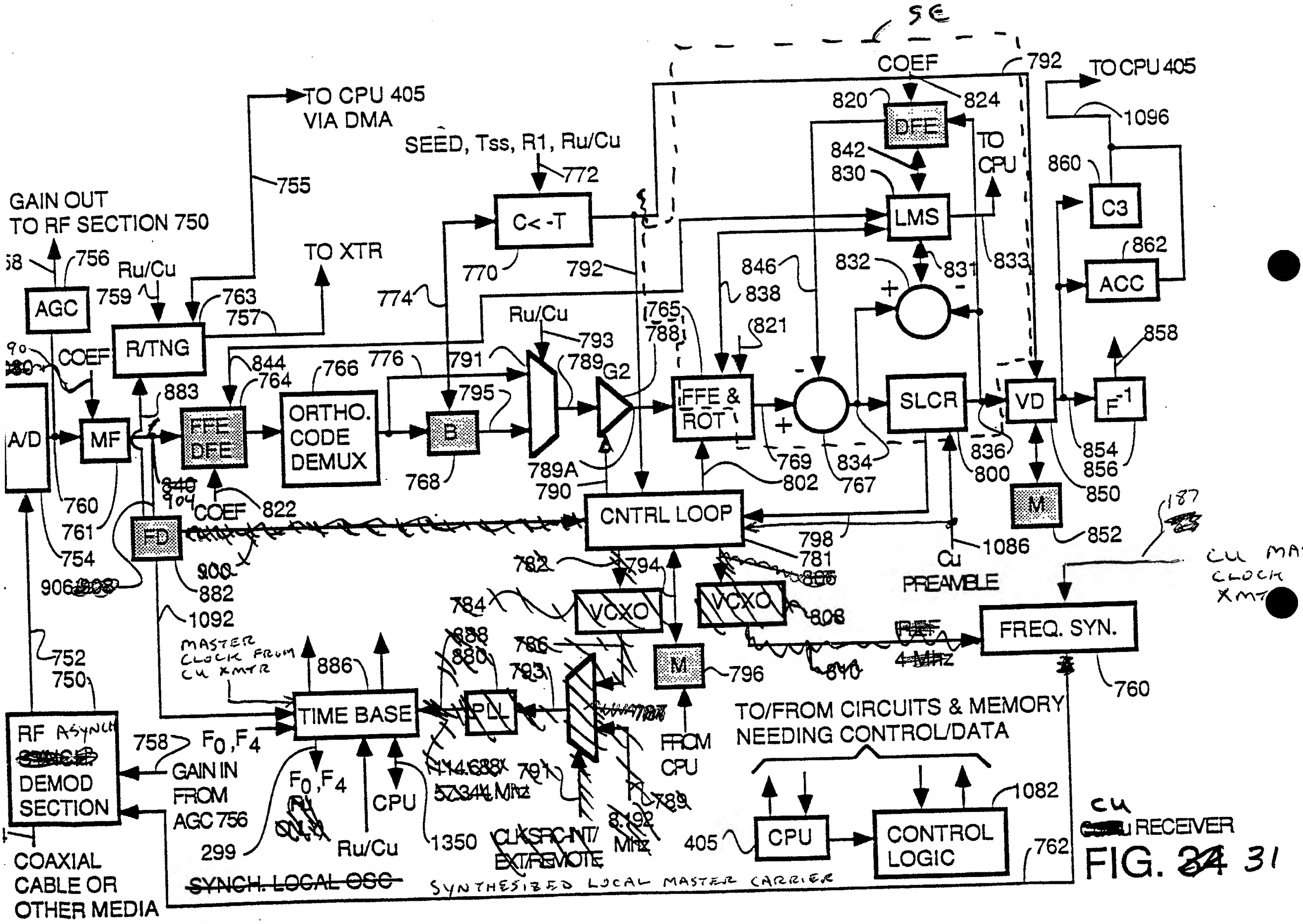

5E
COEF
792
TO CPU 405
820
824
DFE
1096
TO CPU 405 VIA DMA
SEED, Tss, R1, Ru/Cu
772
842
830
TO CPU
860
C3
755
GAIN OUT TO RF SECTION 750
C<-T
LMS
TO XTR
862
ACC
770
792
846
832
831
833
774
838
765
788
821
Ru/Cu
793
858
AGC
759
763
757
R/TNG
776
791
789
G2
844
764
766
795
883
FFE DFE
ORTHO. CODE DEMUX
FFE & ROT
SLCR
VD
F-1
A/D
MF
B
769
834
836
800
854
856
850
789A
768
802
767
790
M
852
760
761
754
906
COEF
822
CNTRL LOOP
798
781
1086
Cu PREAMBLE
FD
900
882
1092
782
794
784
VCXO
VCXO
808
FREQ. SYN.
4 MHz
752
750
MASTER CLOCK FROM CU XMTR
886
786
793
796
840
760
TIME BASE
PLL
M
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
RF ASYNCH DEMOD SECTION
758
F0,F4
GAIN IN FROM AGC 756
FROM CPU
791
789
1082
CPU
CONTROL LOGIC
405
762
299
Ru/Cu
1350
CLKSRC-INT/ EXT/REMOTE
8.192 MHz
SYNCH. LOCAL OSC
SYNTHESIZED LOCAL MASTER CARRIER
COAXIAL CABLE OR OTHER MEDIA
CU RECEIVER

FIG. 34 31

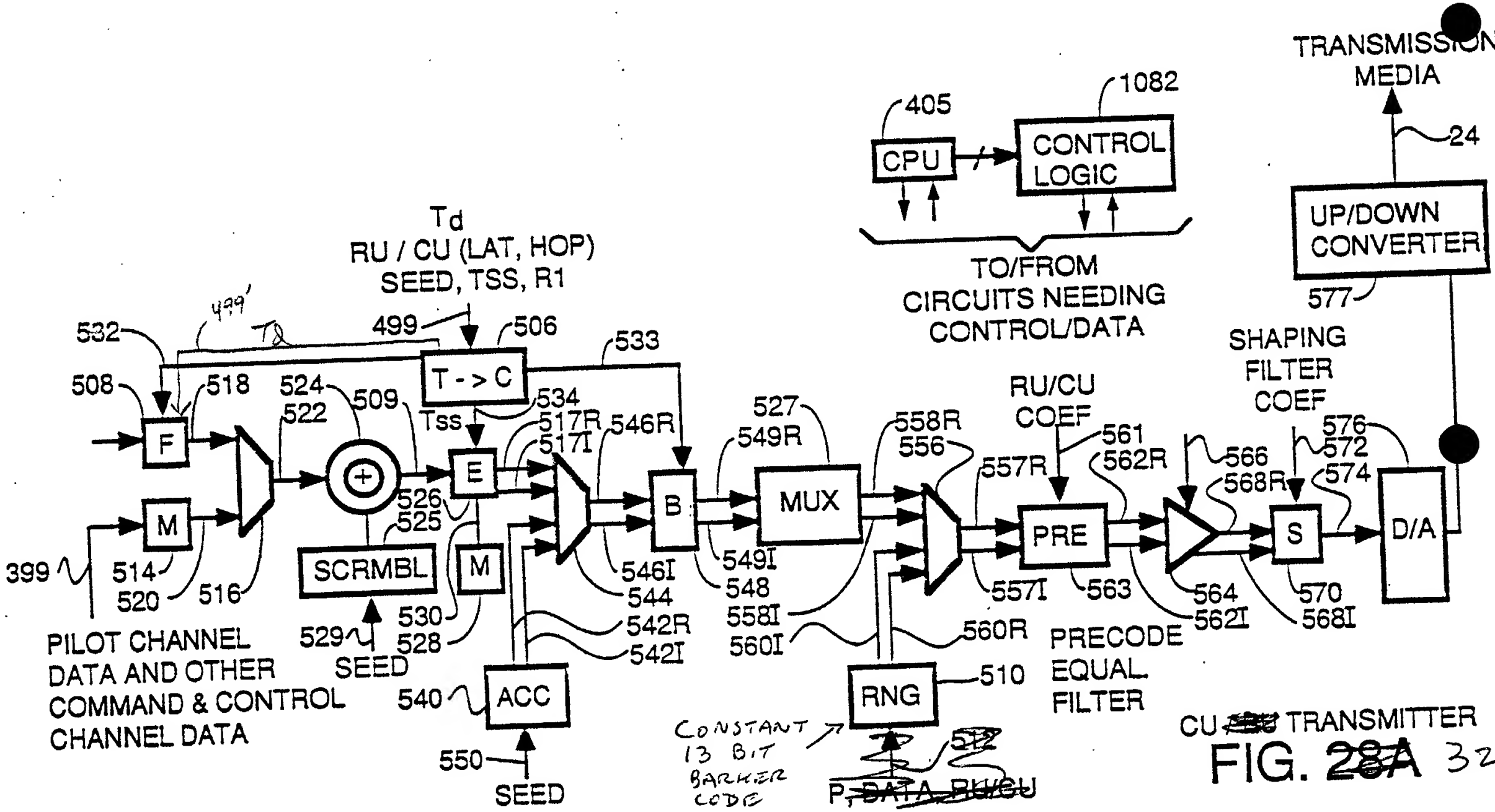

TRANSMISSION MEDIA
24
1082
405
CPU
CONTROL LOGIC
TO/FROM CIRCUITS NEEDING CONTROL/DATA
UP/DOWN CONVERTER
577
Td
RU / CU (LAT, HOP)
SEED, TSS, R1
499'
Td
499
506
T -> C
533
532
508
518
524
522
509
Tss
534
517R
517I
546R
527
549R
558R
556
RU/CU COEF
561
562R
557R
566
568R
576
572
574
SHAPING FILTER COEF
F
M
E
B
MUX
PRE
S
D/A
526
525
546I
544
549I
548
558I
560I
542R
542I
560R
557I
563
564
562I
570
568I
399
514
520
516
SCRMBL
M
530
528
529
SEED
PILOT CHANNEL DATA AND OTHER COMMAND & CONTROL CHANNEL DATA
540
ACC
550
SEED
RNG
510
CONSTANT 13 BIT BARKER CODE
PRECODE EQUAL FILTER
CU TRANSMITTER

FIG. 28A

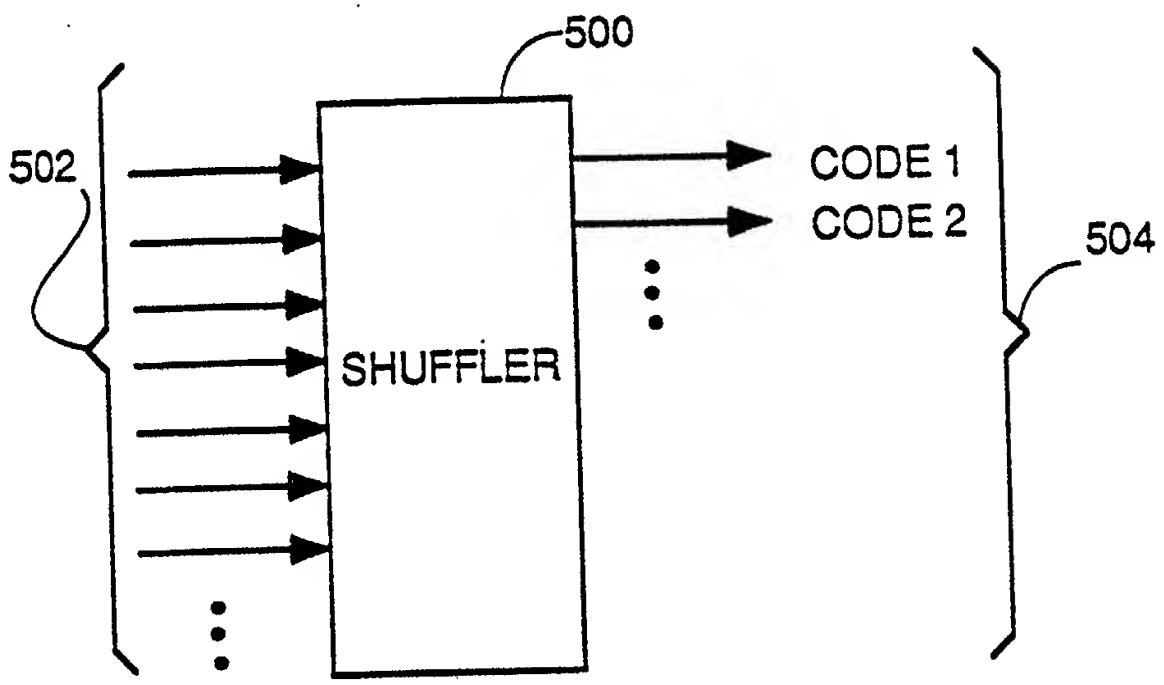


FIG. 27 38

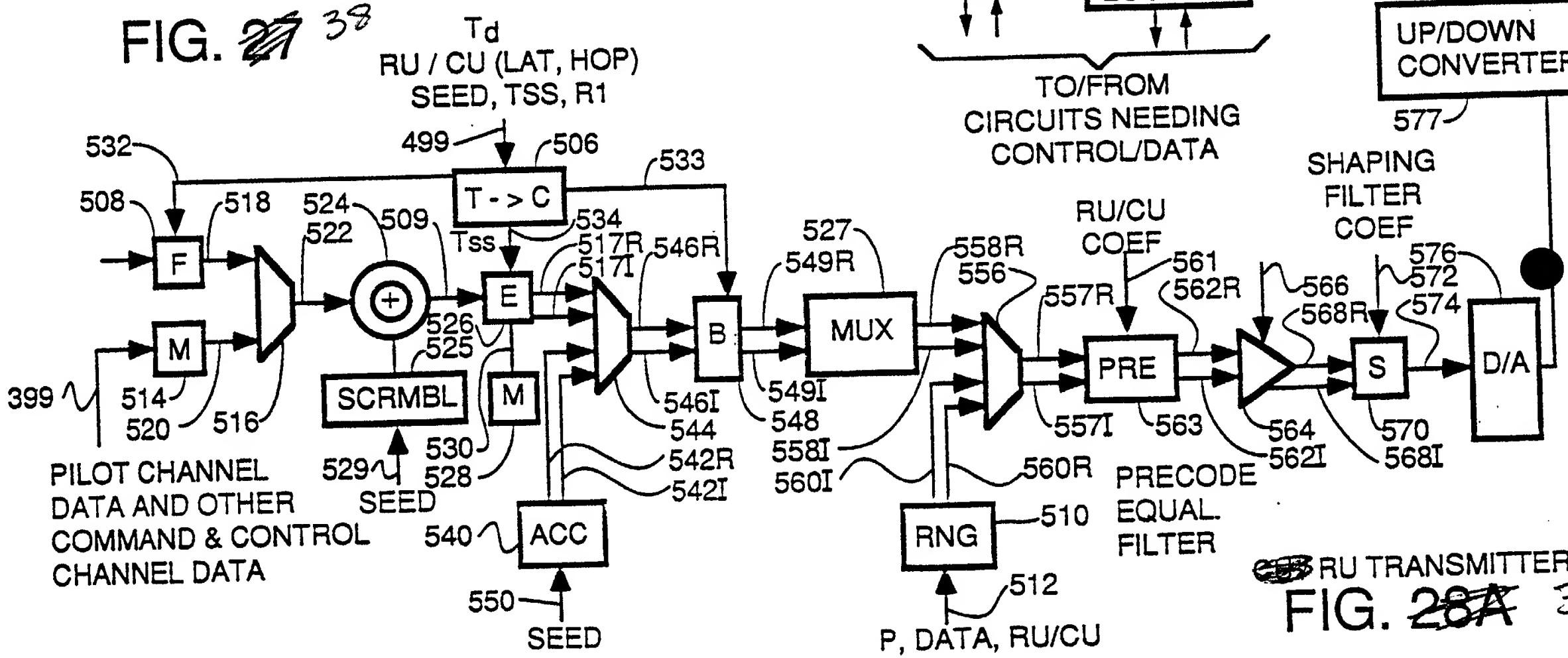
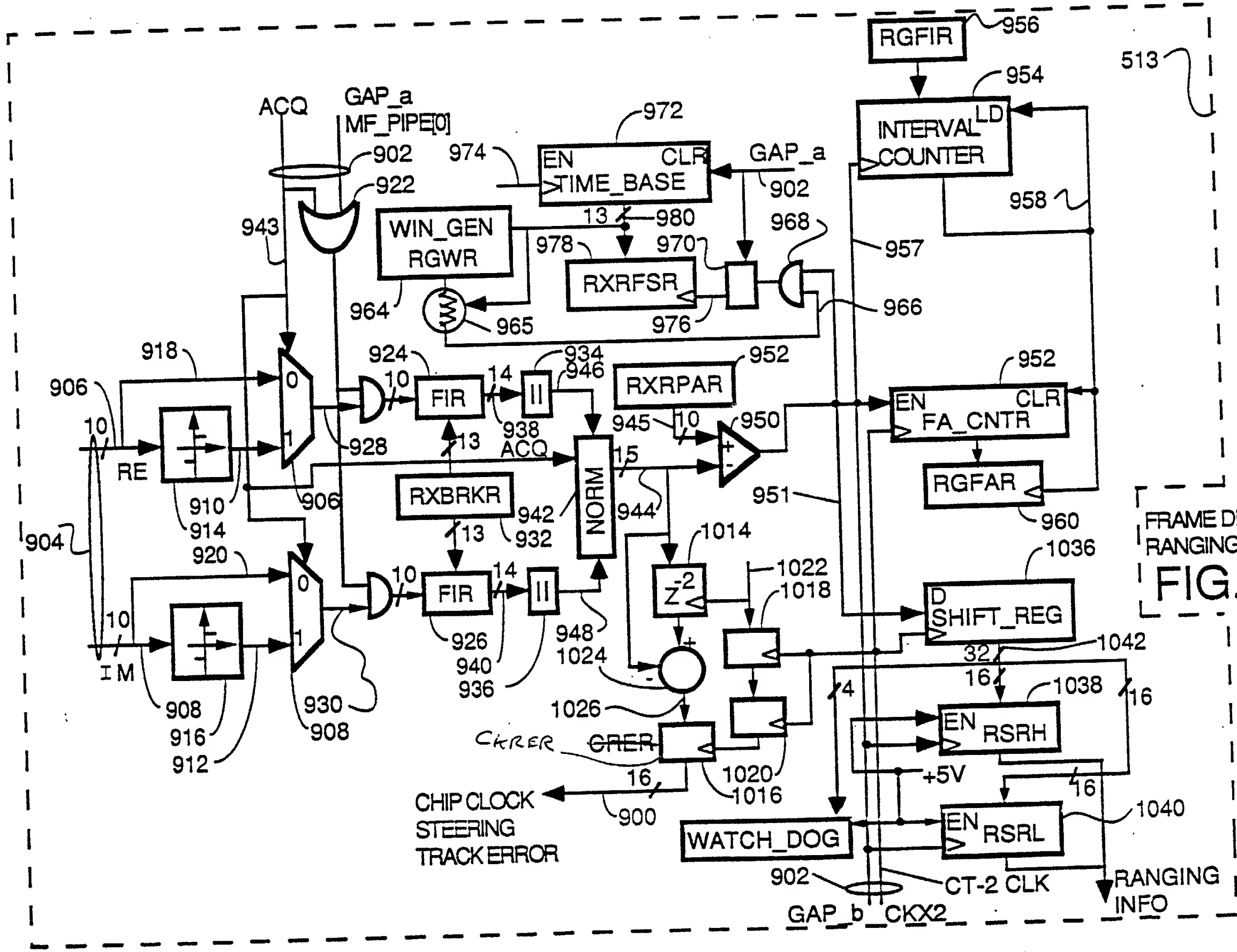


FIG. 28A 3


RGFIR
956
513
954
INTERVAL COUNTER
LD
ACQ
GAP_a
MF_PIPE[0]
902
922
943
974
EN
CLR
TIME_BASE
972
GAP_a
902
958
957
968
WIN_GEN
RGWR
13
980
978
970
RXRFSR
964
965
976
966
918
906
924
934
946
952
RXRPAR
952
10
14
FIR
II
EN
CLR
FA_CNTR
945
10
950
938
ACQ
928
13
15
RE
RXBRKR
942
932
NORM
944
951
RGFAR
960
910
914
906
904
920
1014
1036
FRAME DETECTOR/
RANGING DETECTO
FIG. 38
1022
1018
Z-2
D
SHIFT_REG
10
FIR
14
II
926
940
936
948
1024
1042
32
16
4
1038
16
I M
908
916
912
930
908
1026
EN
RSRH
CKRER
GRER
16
1020
1016
+5V
16
CHIP CLOCK
STEERING
TRACK ERROR
900
WATCH_DOG
EN
RSRL
1040
902
CT-2 CLK
RANGING
INFO
GAP_b
CKX2

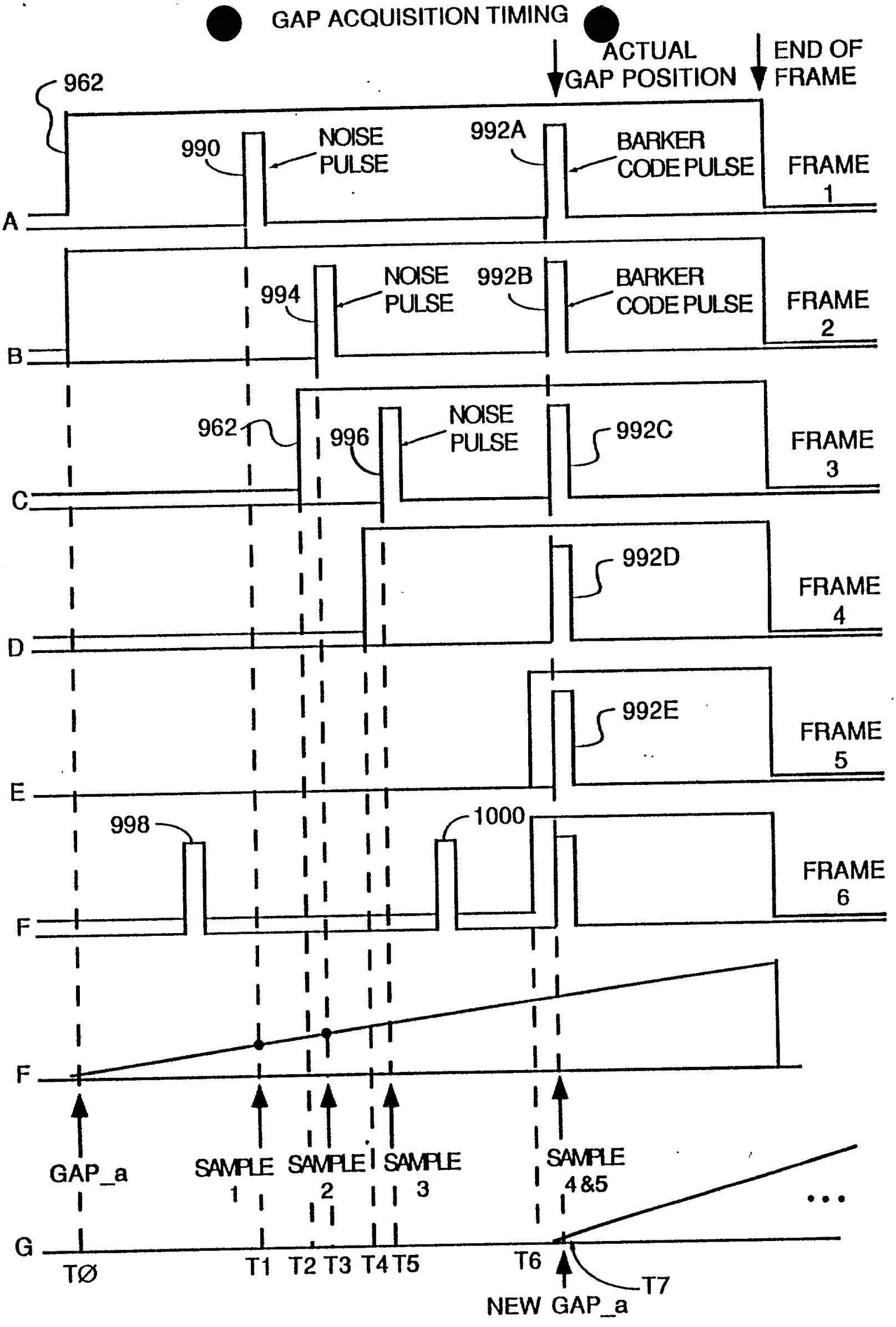
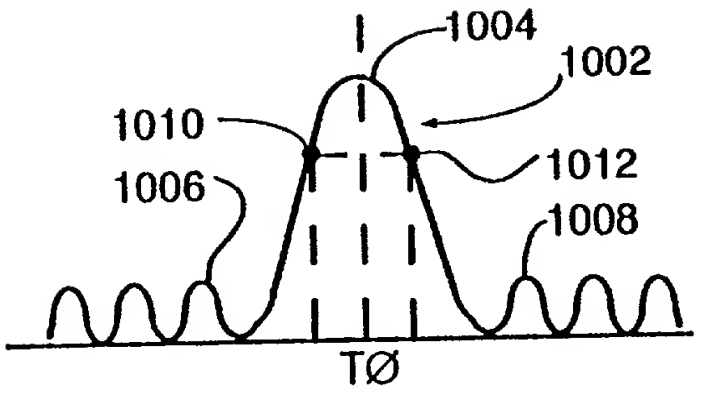
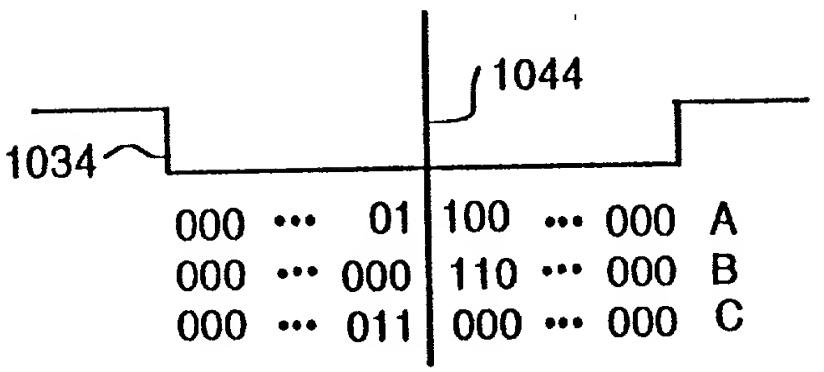

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
...
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 39 35



36

FIG. 40

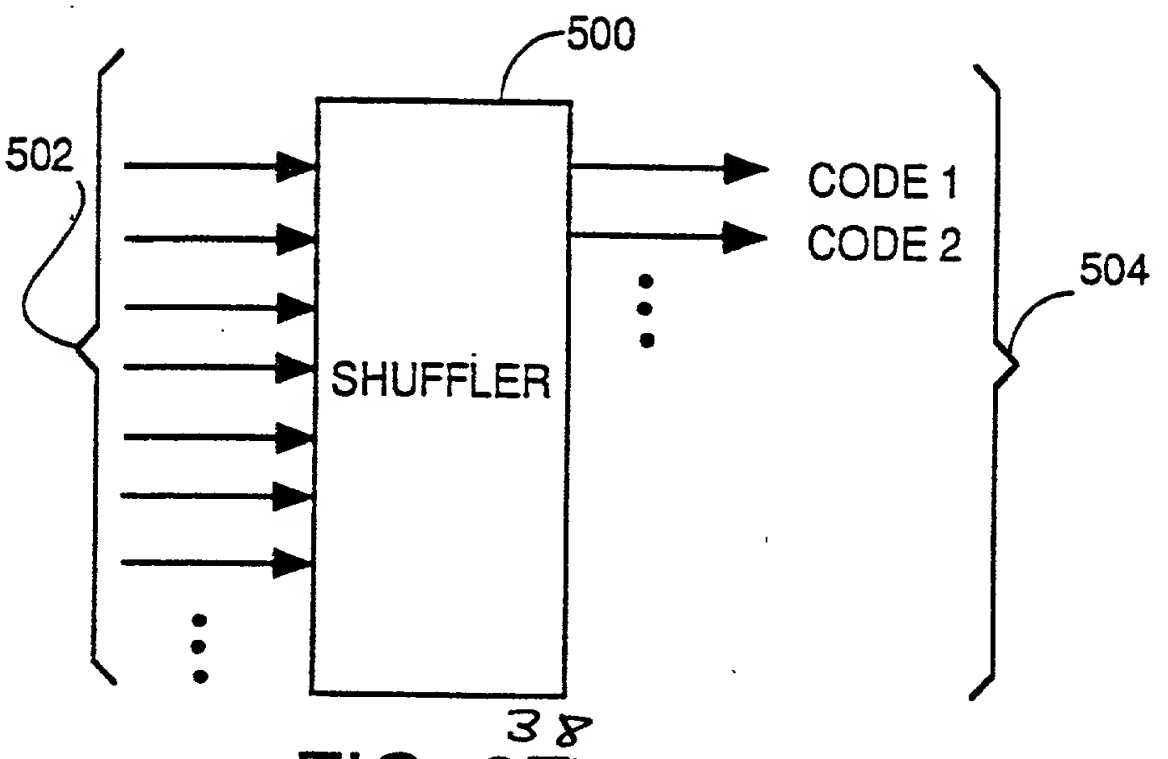


000	•••	01	100	•••	000	A
000	•••	000	110	•••	000	B
000	•••	011	000	•••	000	C

37

FIG. 41

FINE TUNING TO CENTER BARKER CODE



38

FIG. 27

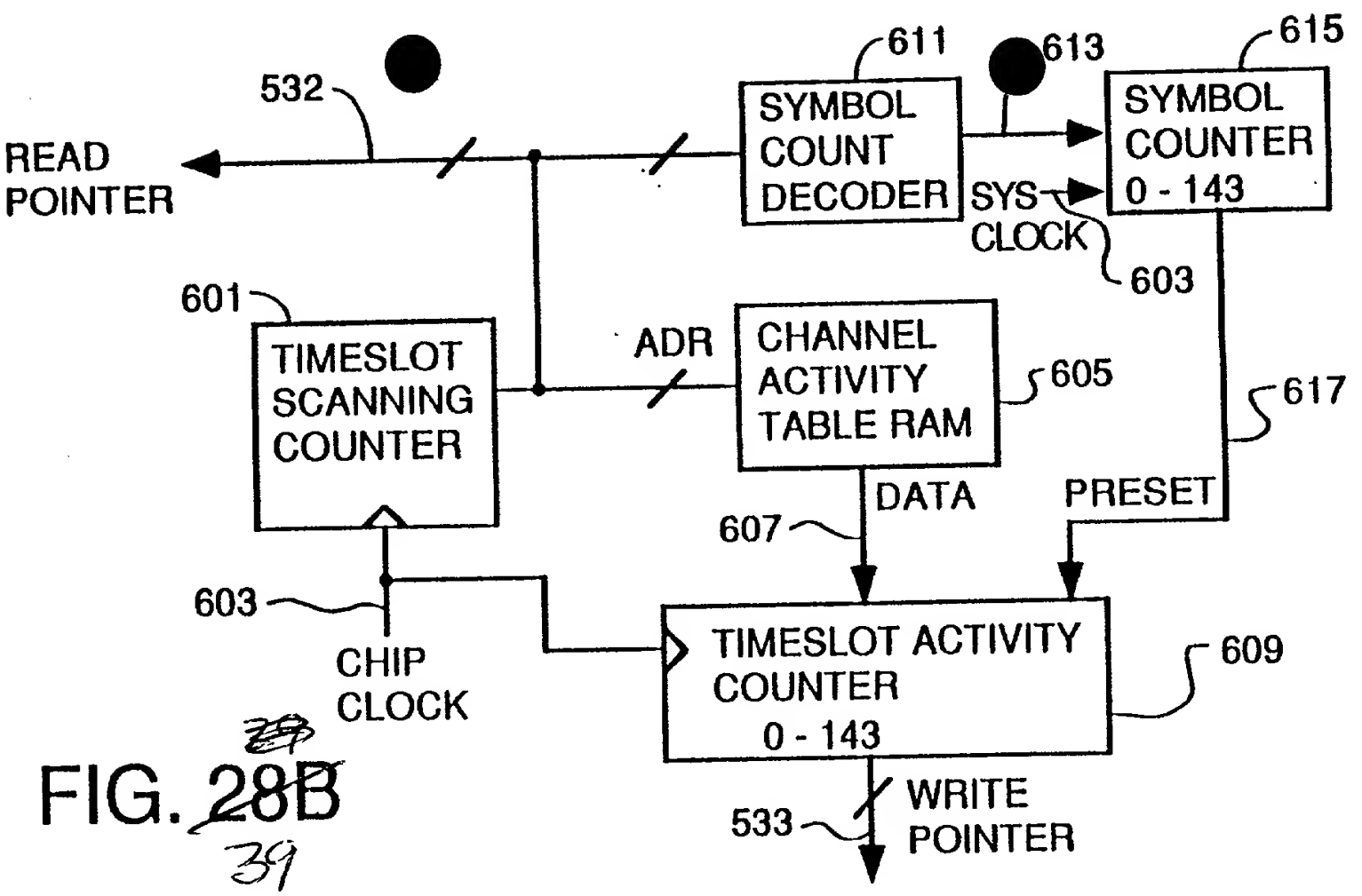


FIG. 28B

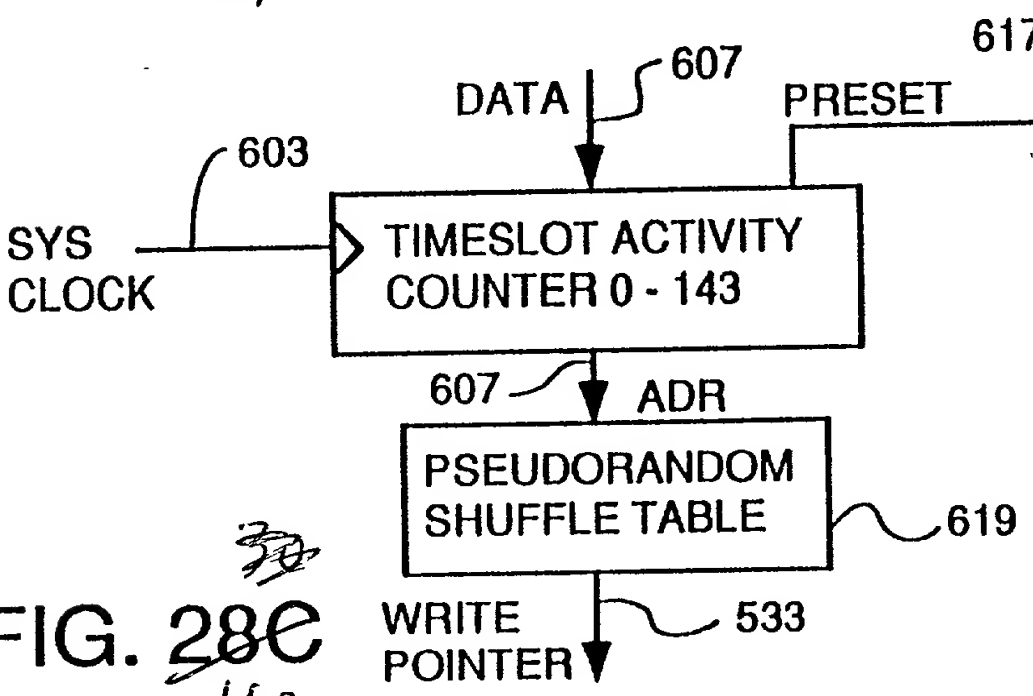


FIG. 28C

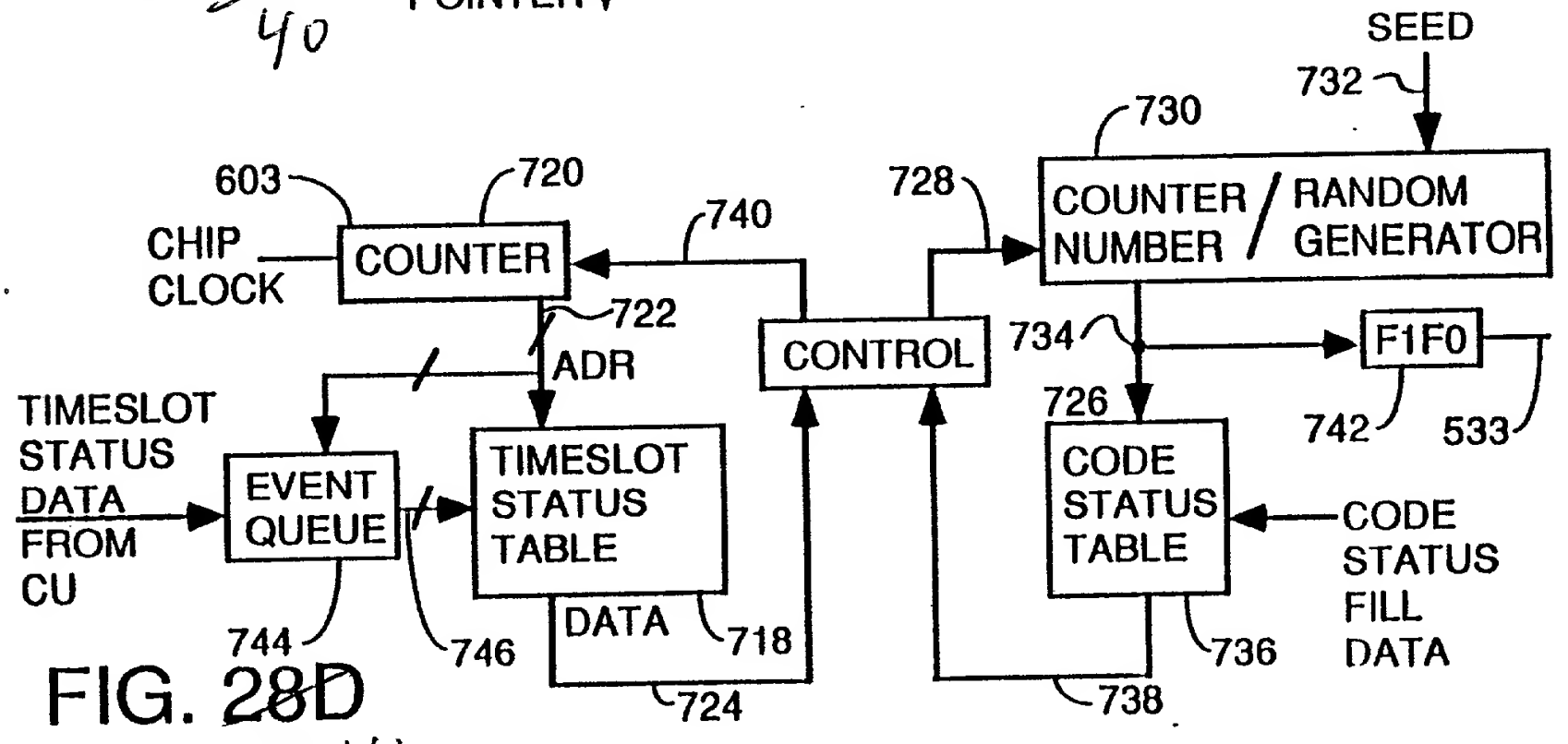
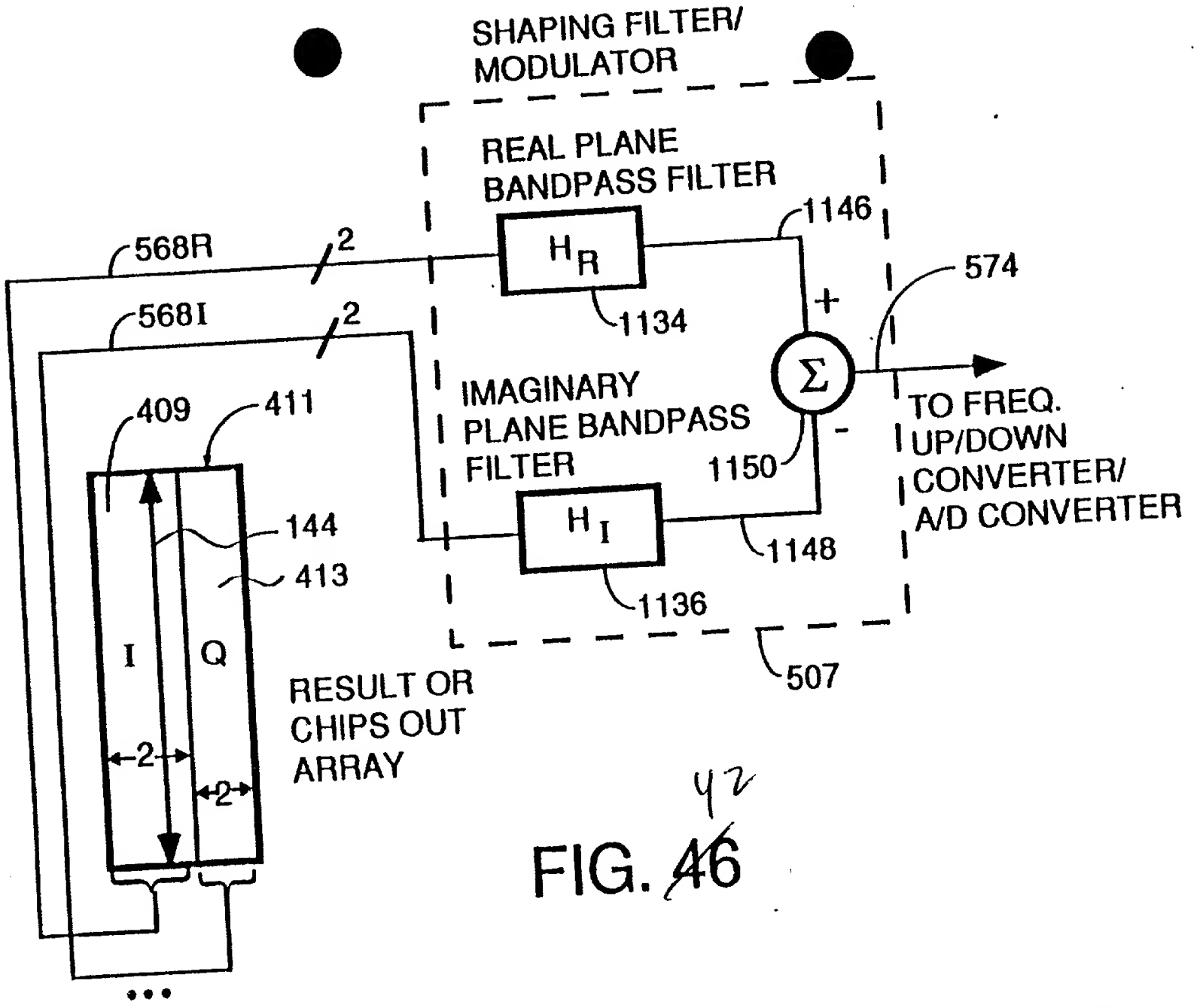
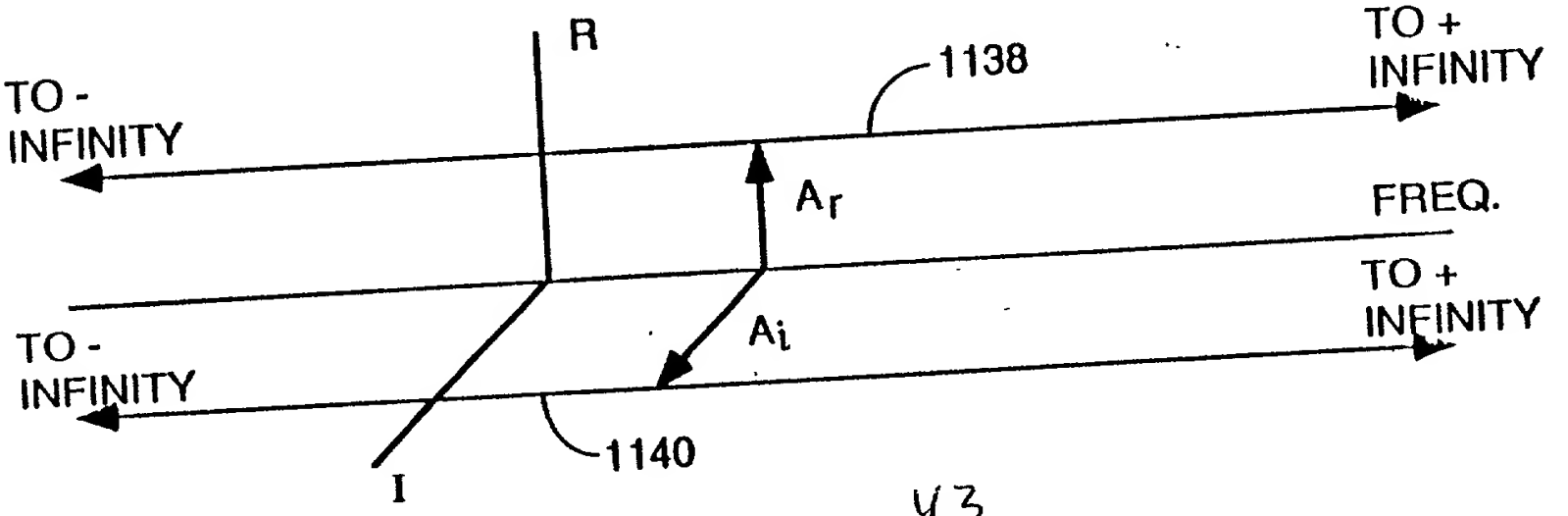


FIG. 28D



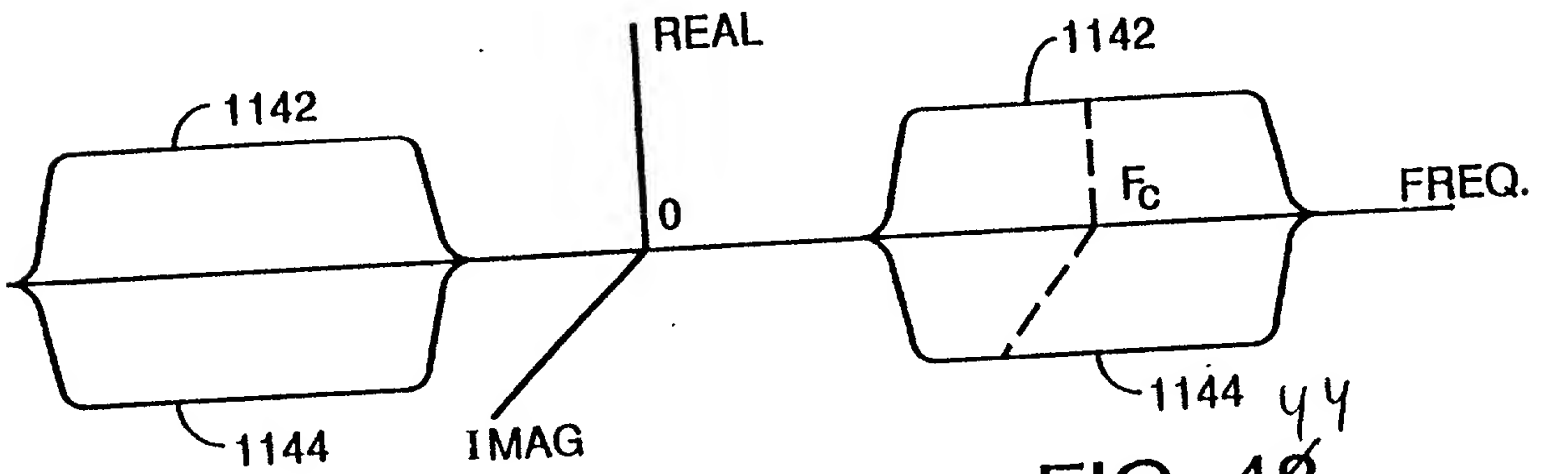
42

FIG. 46



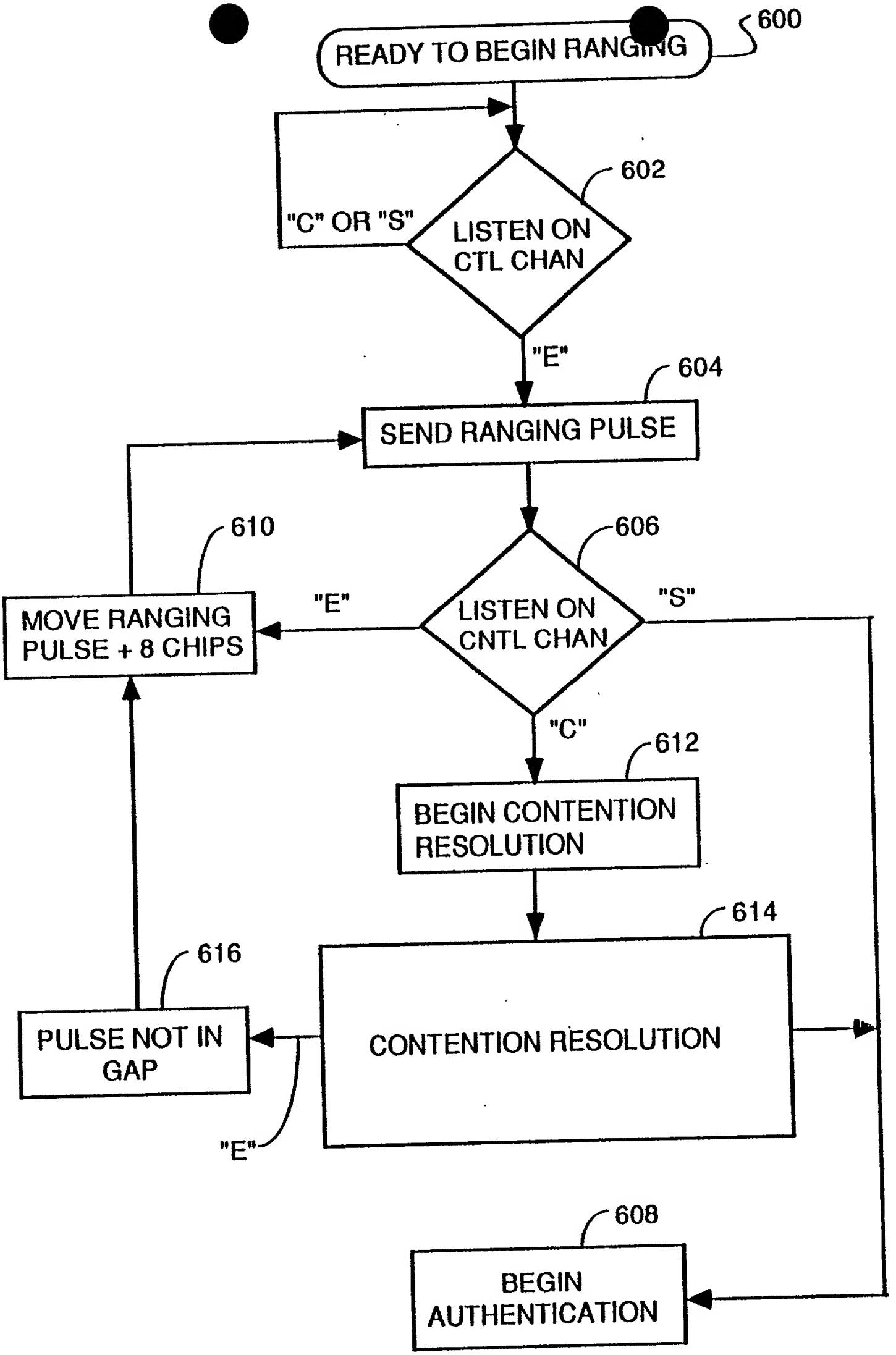
43

FIG. 47



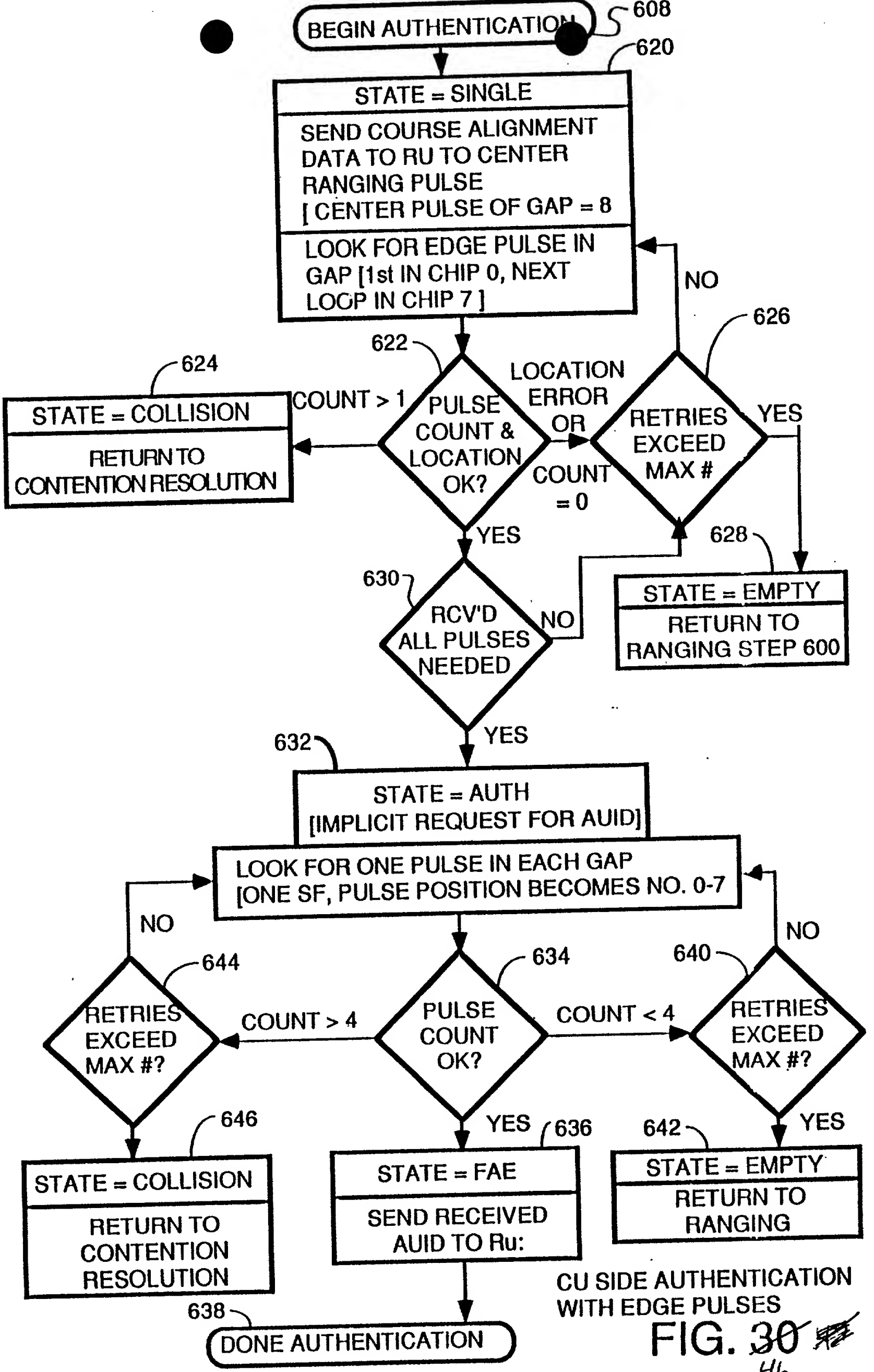
44

FIG. 48



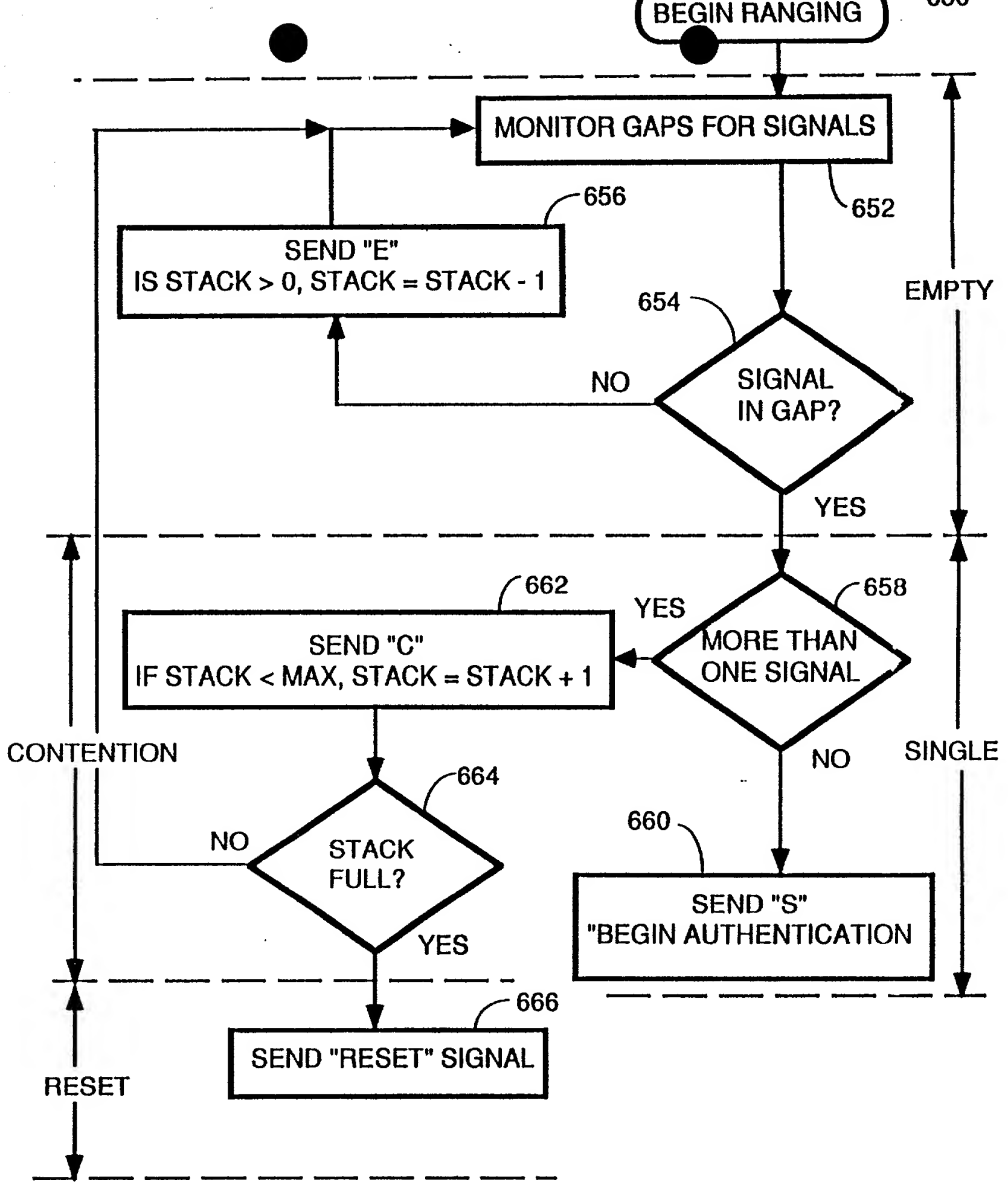
RU RANGING

FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30

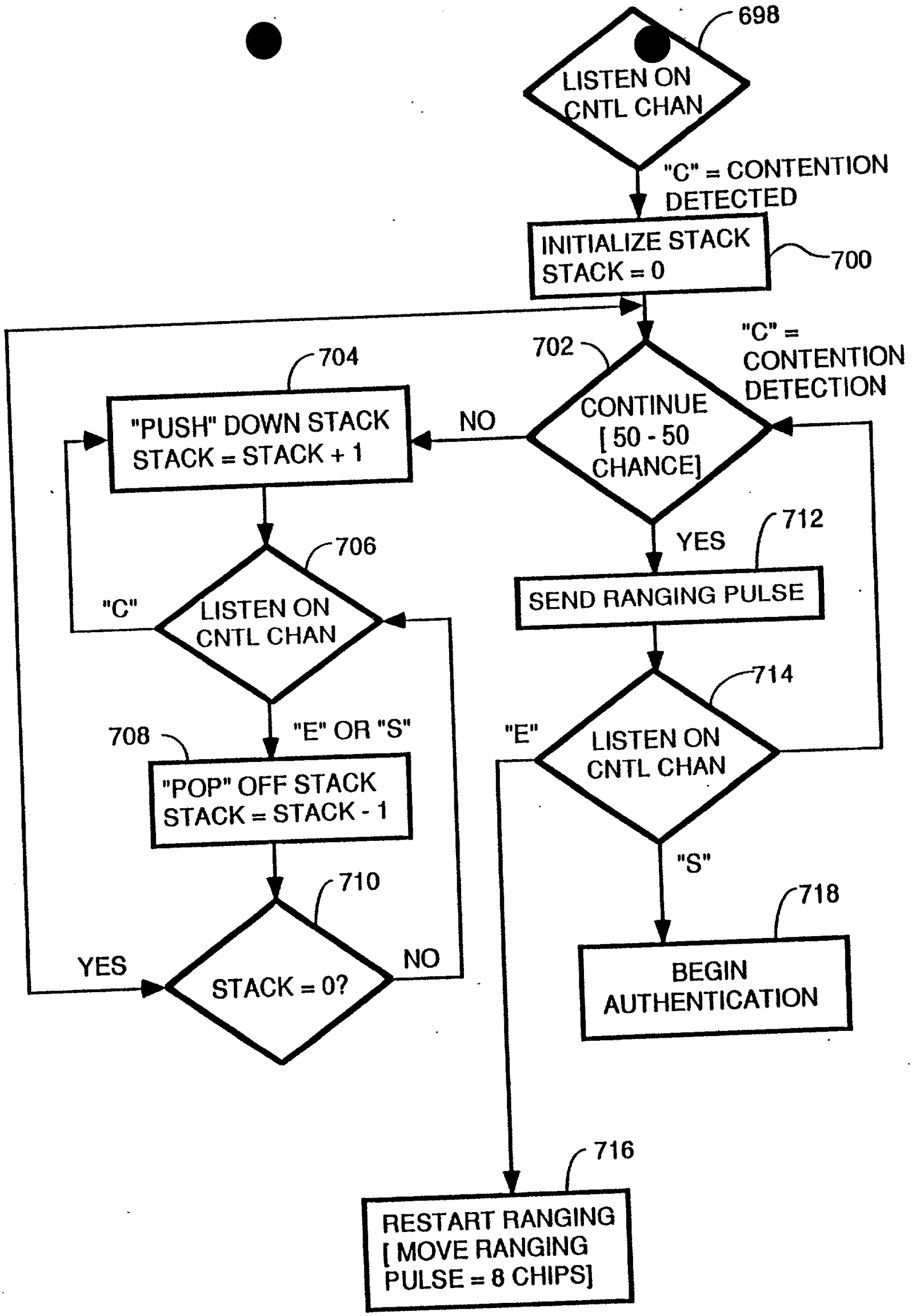


CU RANGING & CONTENTION RESOLUTION

~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

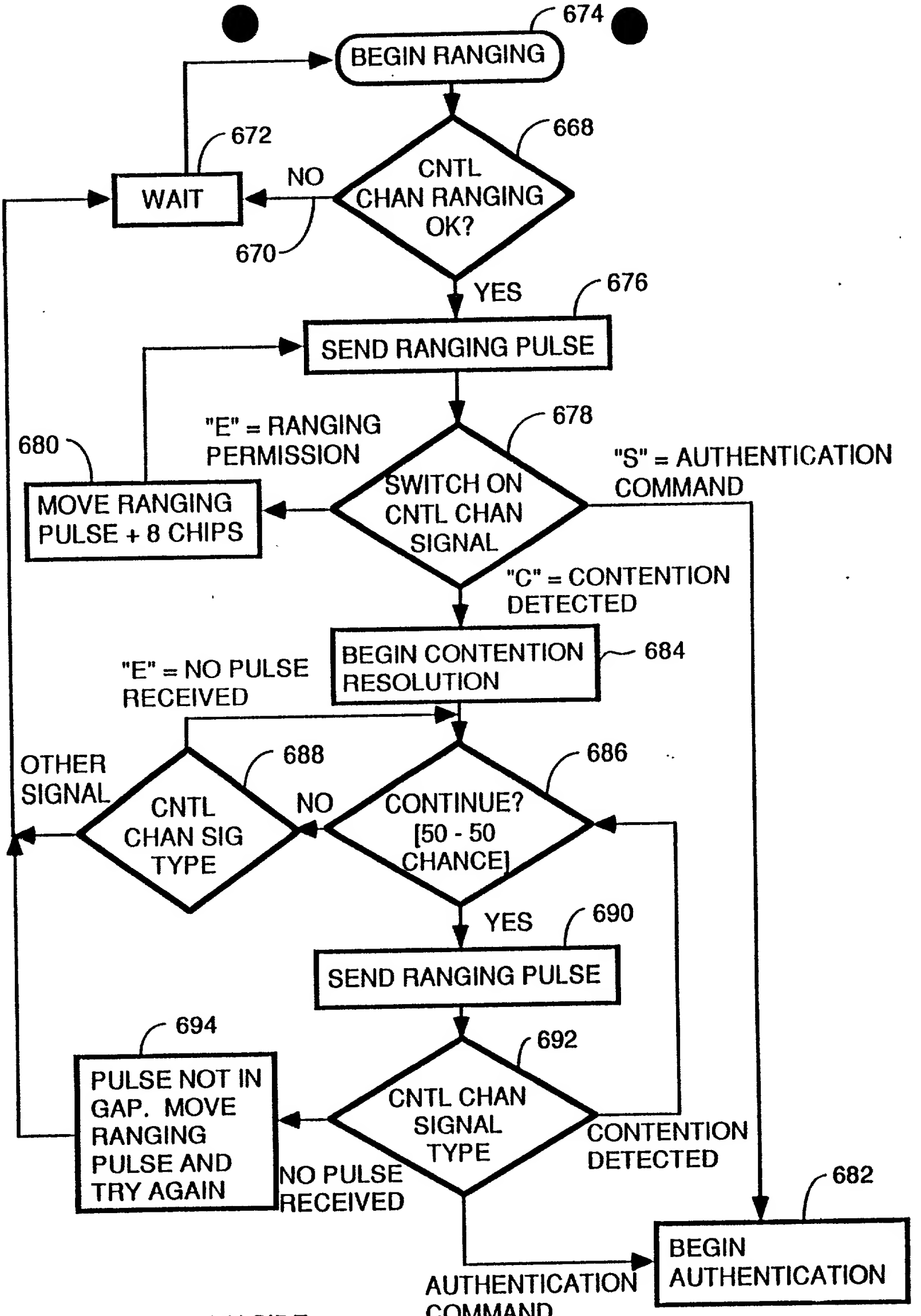
FIG. 31 48

41



CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. 33



RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. 32

50

49

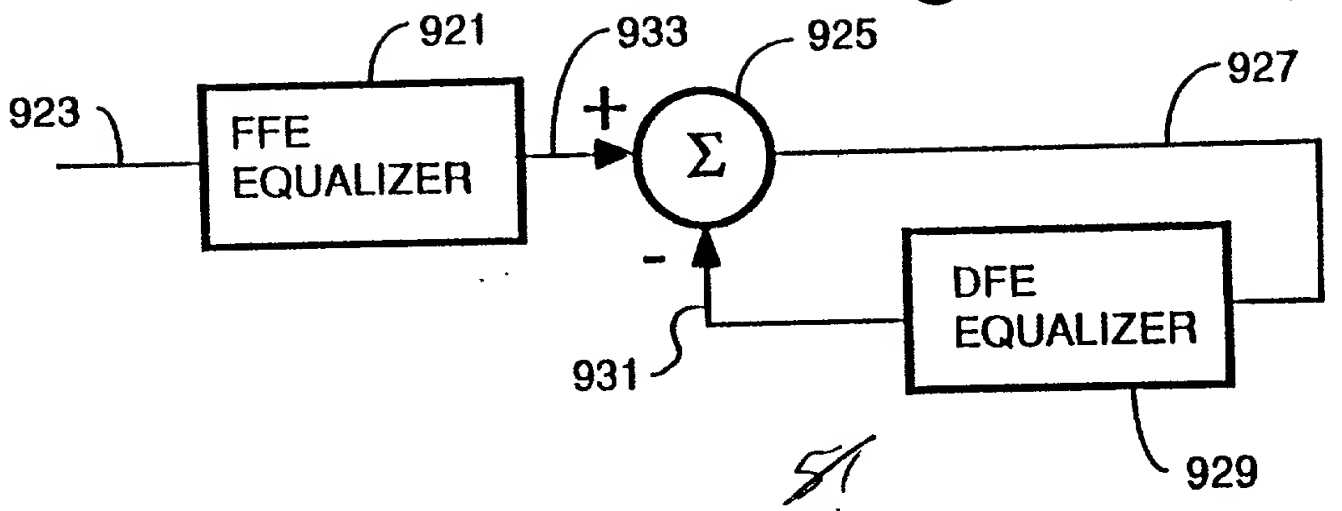


FIG. 37

50

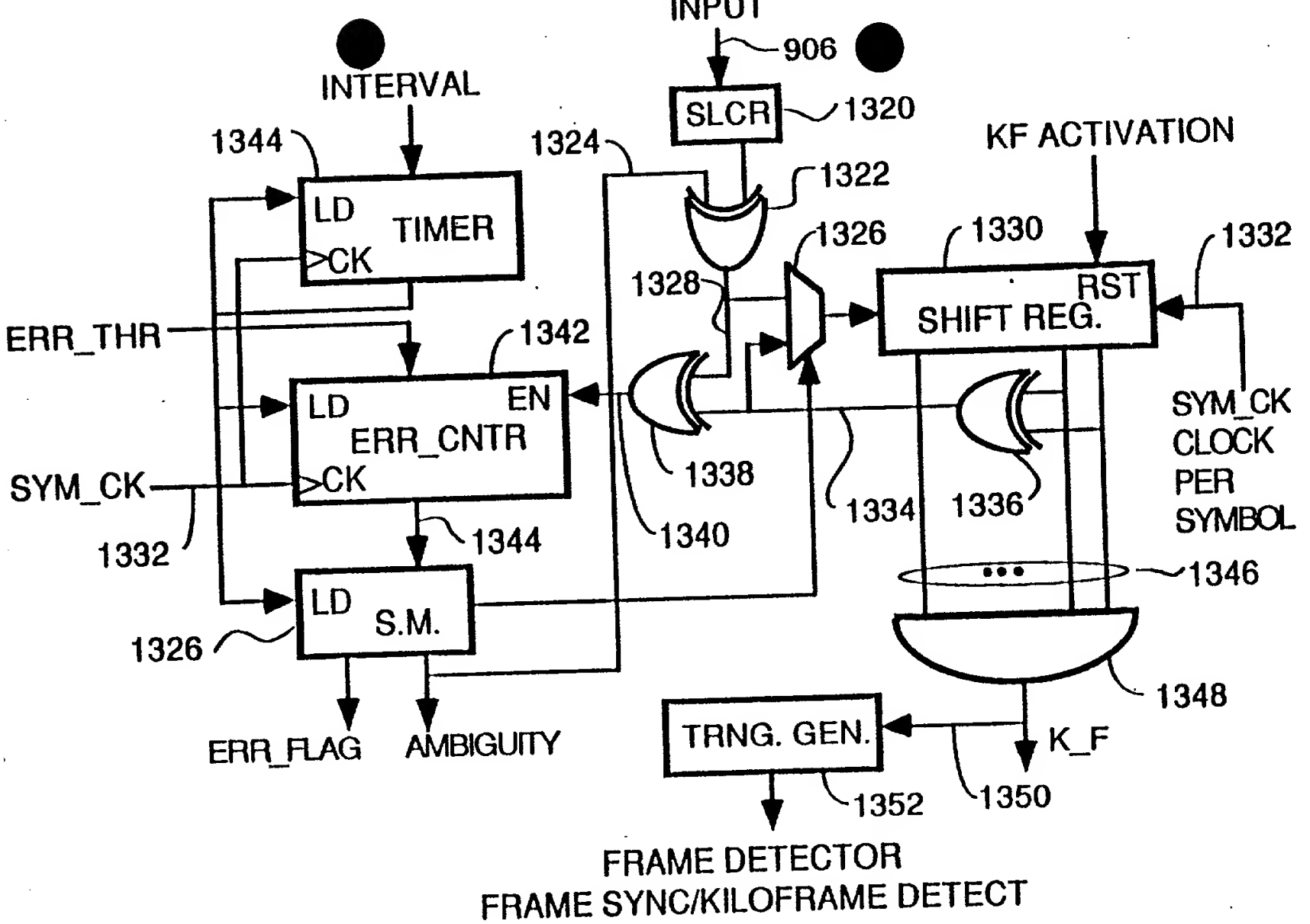
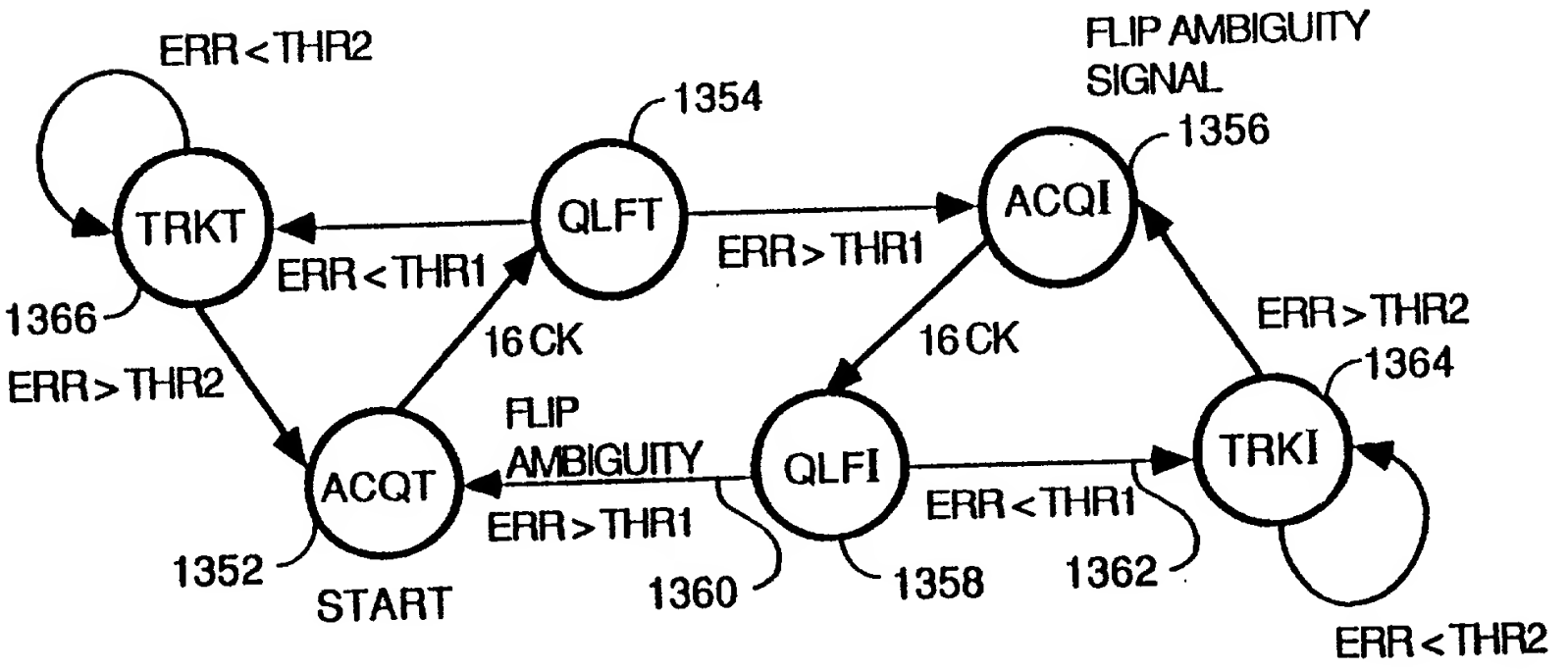


FIG. 52

51



STATE MACHINE

FIG. 53

52

EQUALIZATION TRAINING ALGORITHM

1101

~~1100~~

RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.

1102

CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES

TIME ALIGN-MENT

1104

IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?

NO

1106

GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU

YES

1108

SET GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4

POWER ALIGNMENT

1110

ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE

1112

SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1

TO FIG. ~~45B~~ 53B

~~54A~~

FIG. ~~45A~~ 53A

UPSTREAM EQUALIZATION

1114

CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.

1116

RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.

1118

CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.

1120

TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.

1122

AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.

1124

RU SETS FINAL FFE & DFE COEFFICIENTS INTO PRECODE FFE/DFE FILTER IN TRANSMITTER.

1126

CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO ONE FOR RECEPTION OF UPSTREAM PAYLOAD DATA.

TO FIG. 45C

FIG. ~~45B~~ 54B

53B

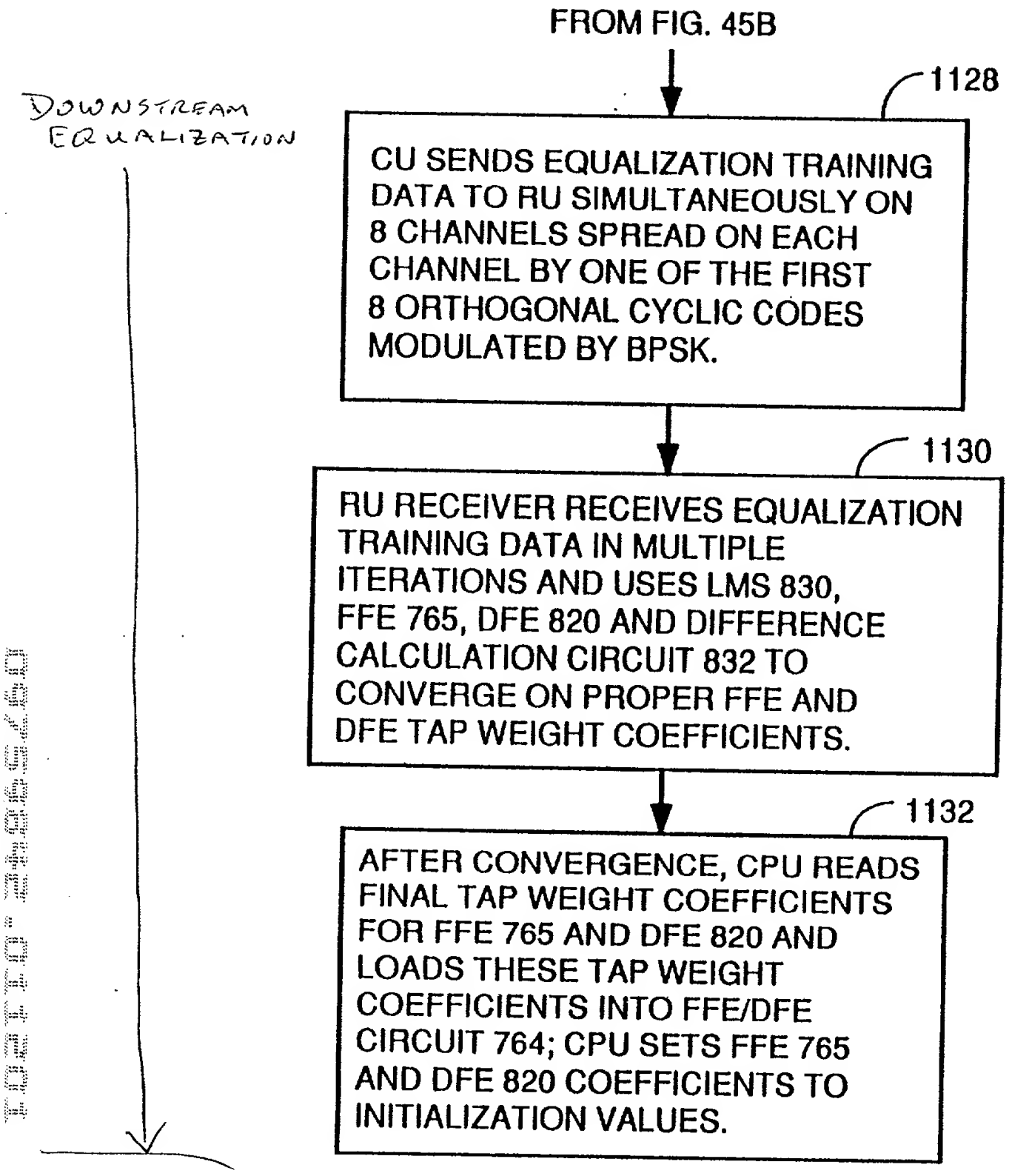


FIG. ~~45C~~ 54C 53C

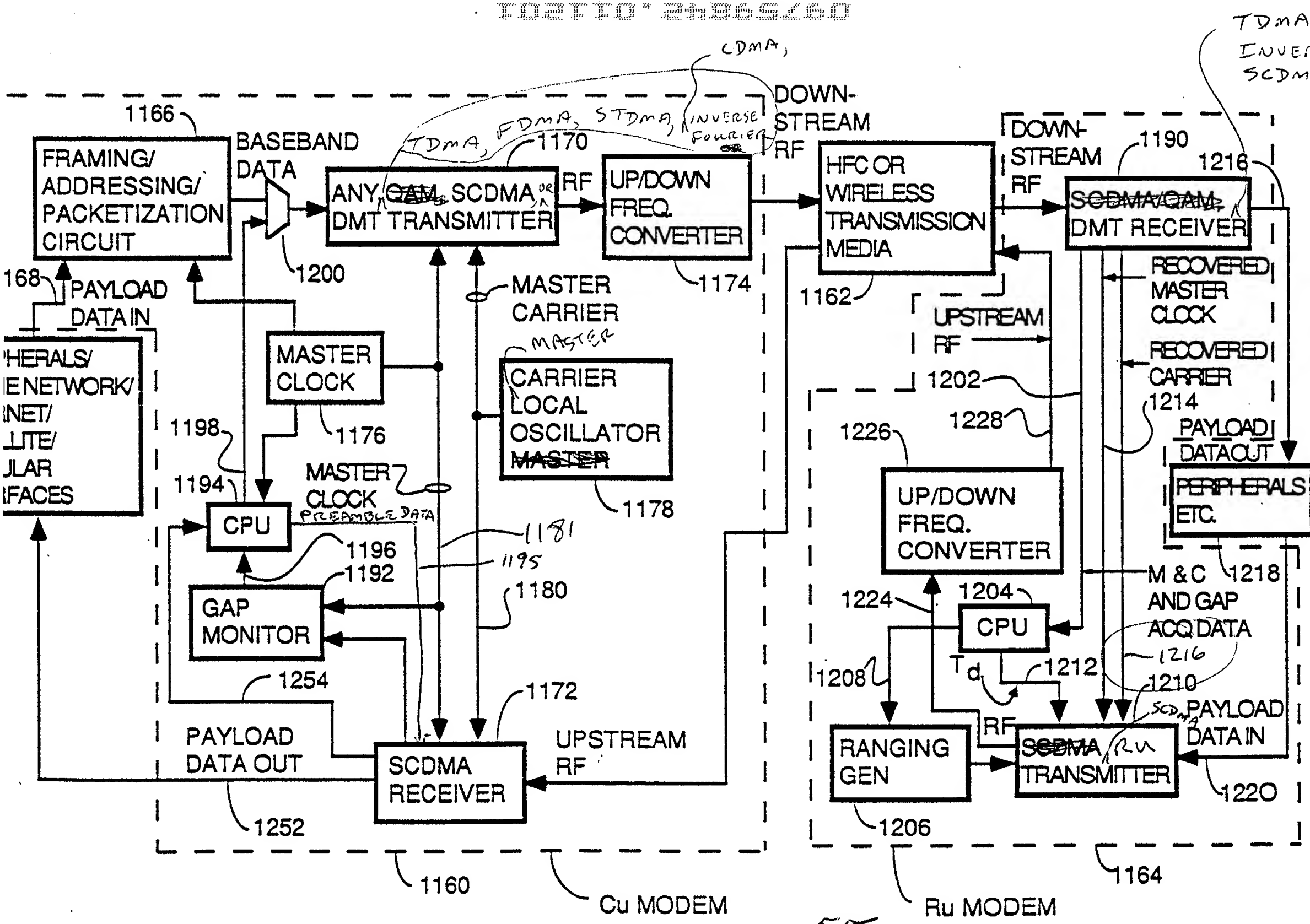
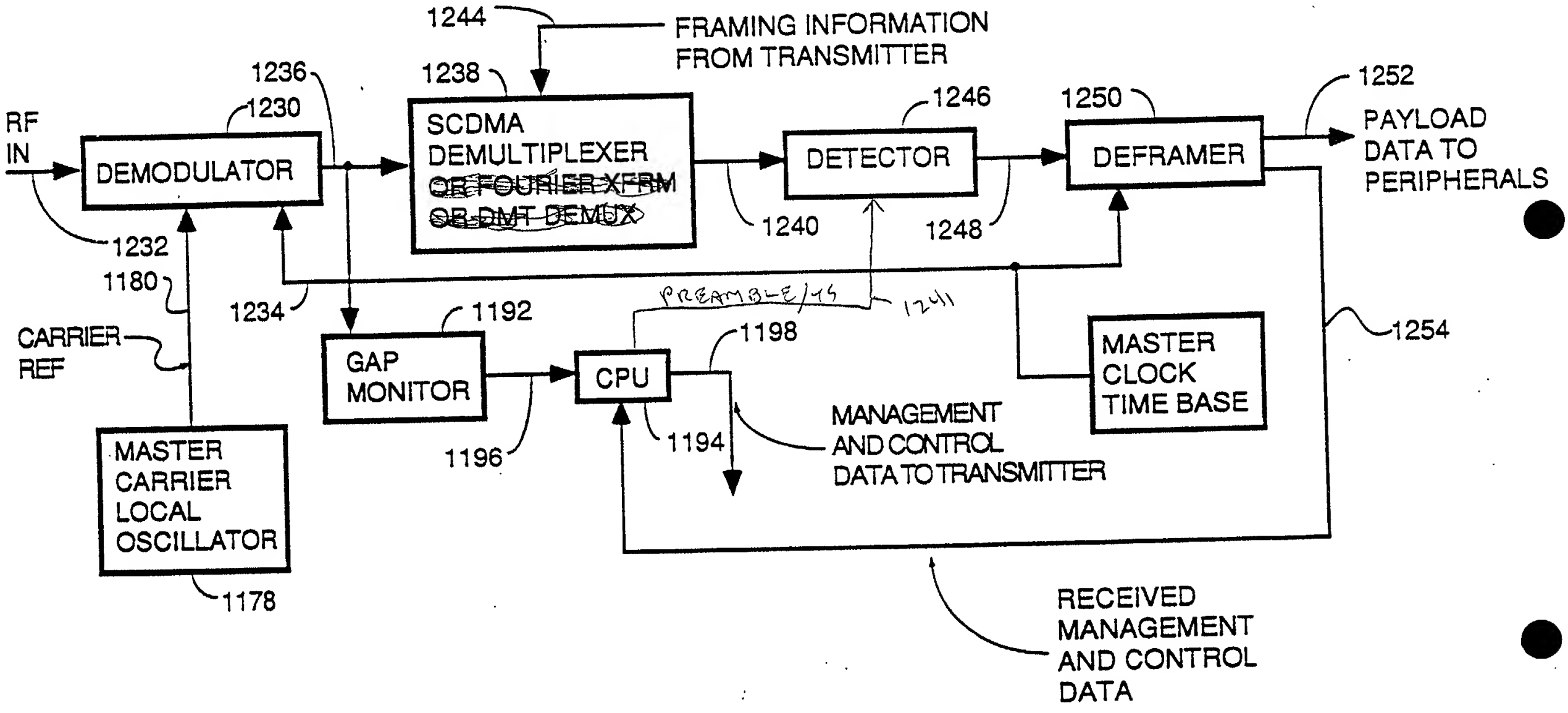

1166
FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
BASEBAND DATA
1200
168
PAYLOAD DATA IN
PERIPHERALS/ NETWORK/ INTERNET/ SATELLITE/ CELLULAR INTERFACES
MASTER CLOCK
1176
1198
1194
CPU
MASTER CLOCK
PREAMBLE DATA
1196
1192
GAP MONITOR
1254
PAYLOAD DATA OUT
1252
1160
Cu MODEM
CDMA,
TDMA, FDMA, STDMA, INVERSE FOURIER OR
1170
ANY, CDMA, SCDMA, OR DMT TRANSMITTER
RF
UP/DOWN FREQ. CONVERTER
1174
MASTER CARRIER
MASTER
CARRIER LOCAL OSCILLATOR MASTER
1178
1181
1195
1180
1172
UPSTREAM RF
SCDMA RECEIVER
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
1162
UPSTREAM RF
1202
1228
1226
UP/DOWN FREQ. CONVERTER
1224
1204
CPU
Td
1212
1208
RANGING GEN
RF
SCDMA TRANSMITTER
1220
1206
Ru MODEM
TDMA, STDMA, INVERSE FOURIER SCDMA, CDMA OR
DOWN-STREAM RF
1190
1216
SCDMA/CDMA DMT RECEIVER
RECOVERED MASTER CLOCK
RECOVERED CARRIER
1214
PAYLOAD DATA OUT
PERIPHERALS ETC.
1218
M &C AND GAP ACQ DATA
1216
1210
SCDMA PAYLOAD DATA IN
1164

FIG. 49

55

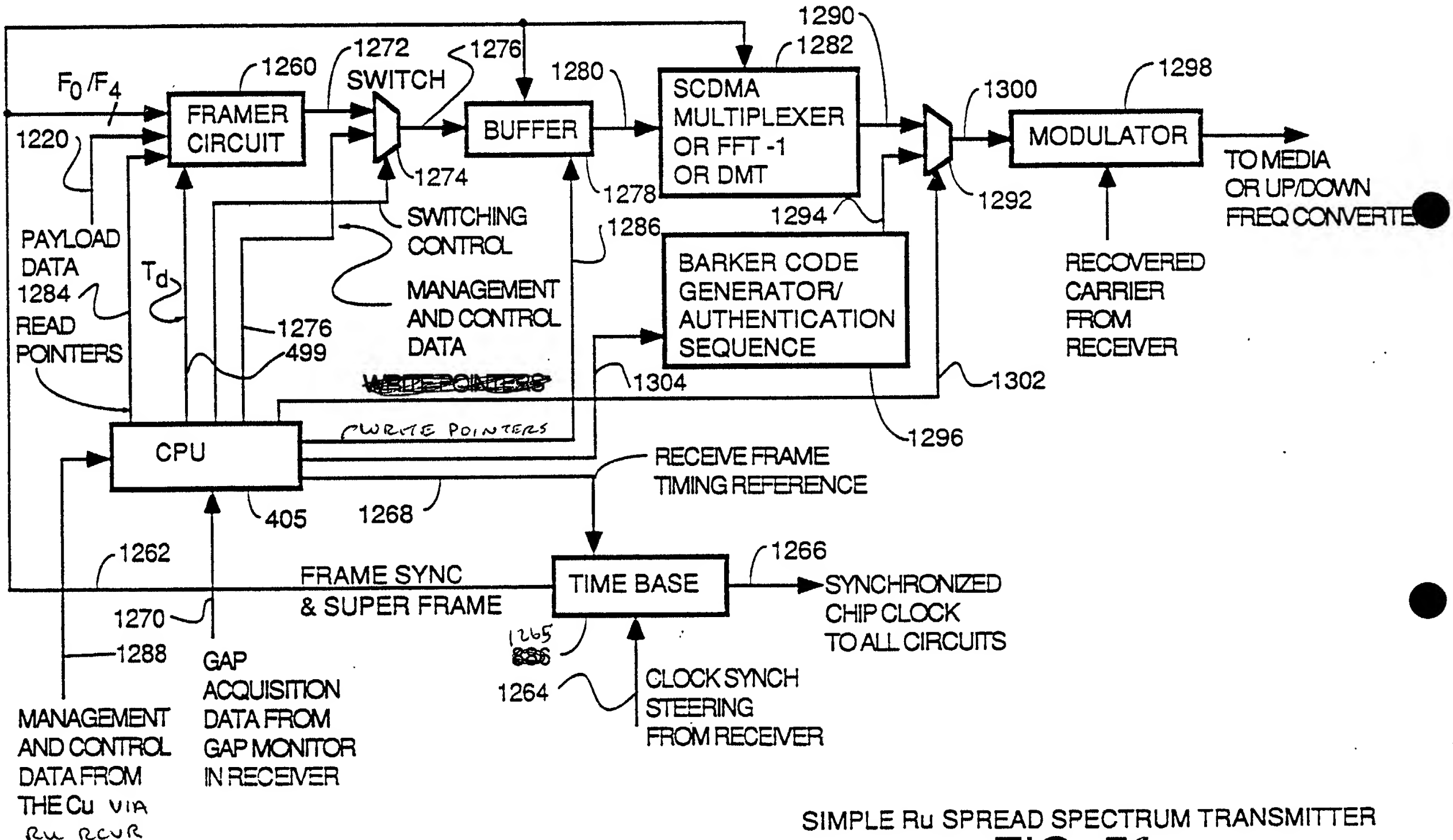
54



SIMPLE Cu SPREAD SPECTRUM RECEIVER

FIG. ~~50~~ 56

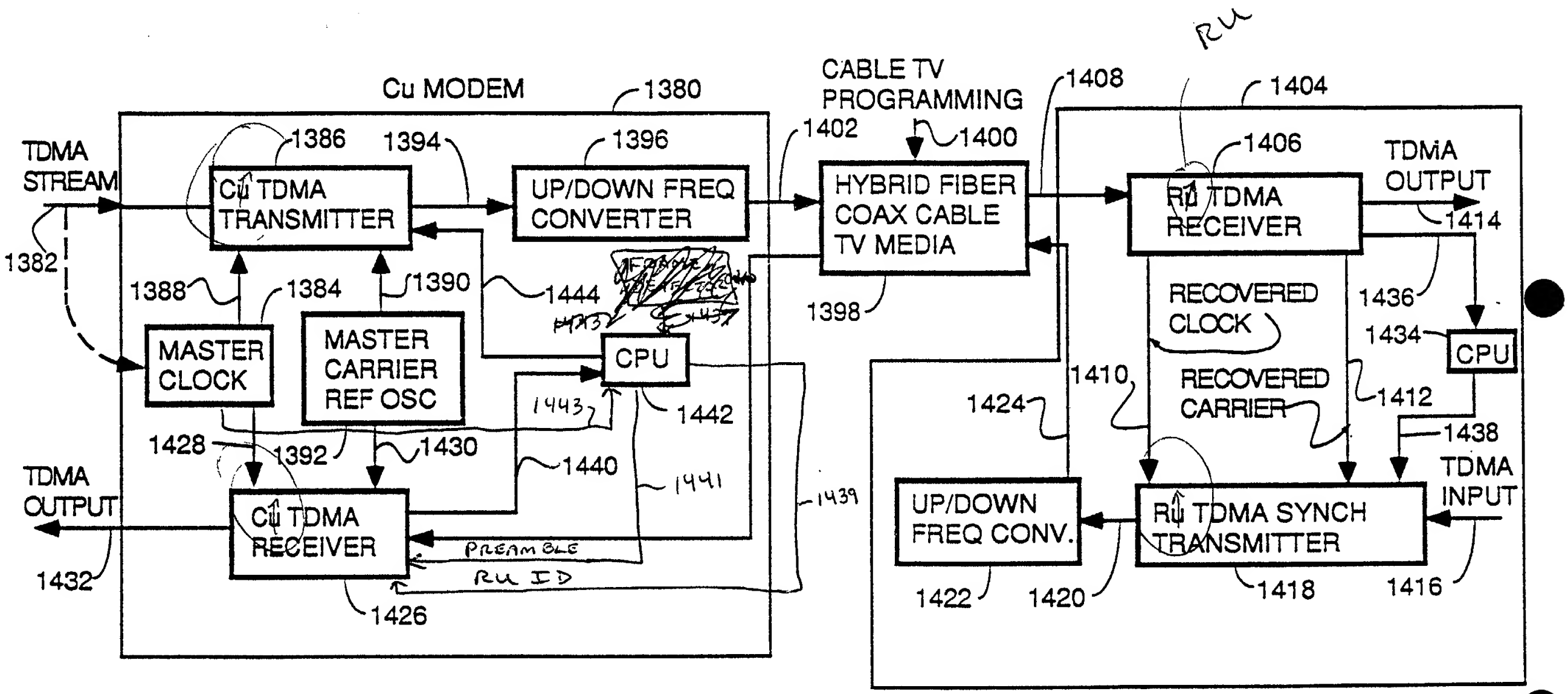
55



SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. 51

56



SYNCHRONOUS TDMA SYSTEM

FIG. ~~54~~ ~~58~~ 57

OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

SE Function

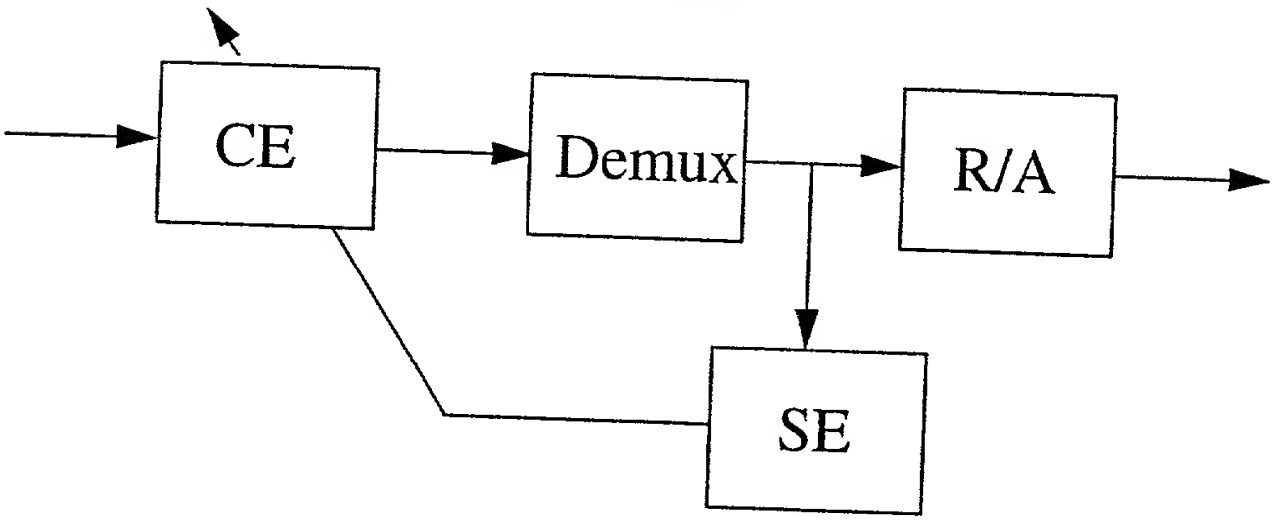
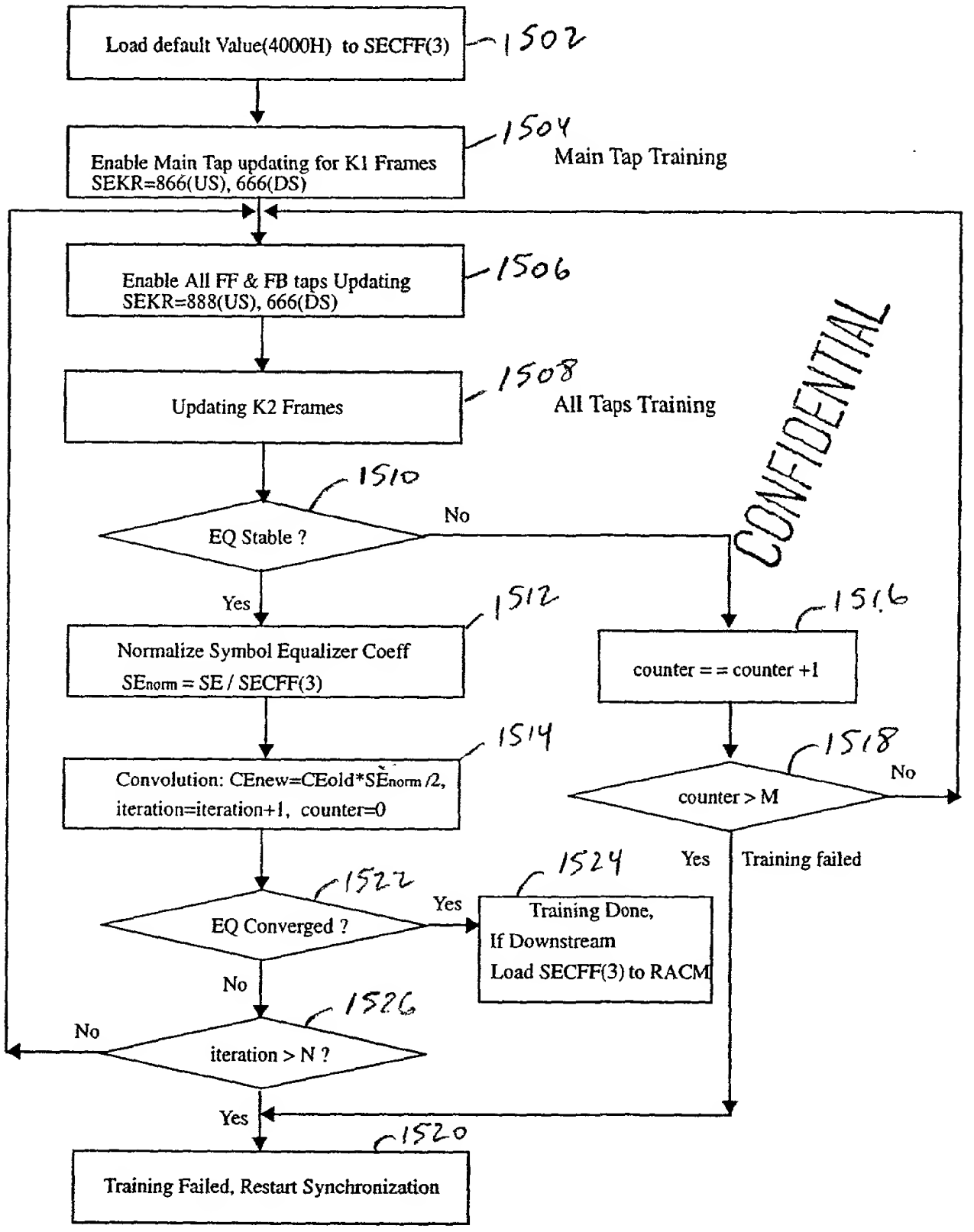


FIG. 59

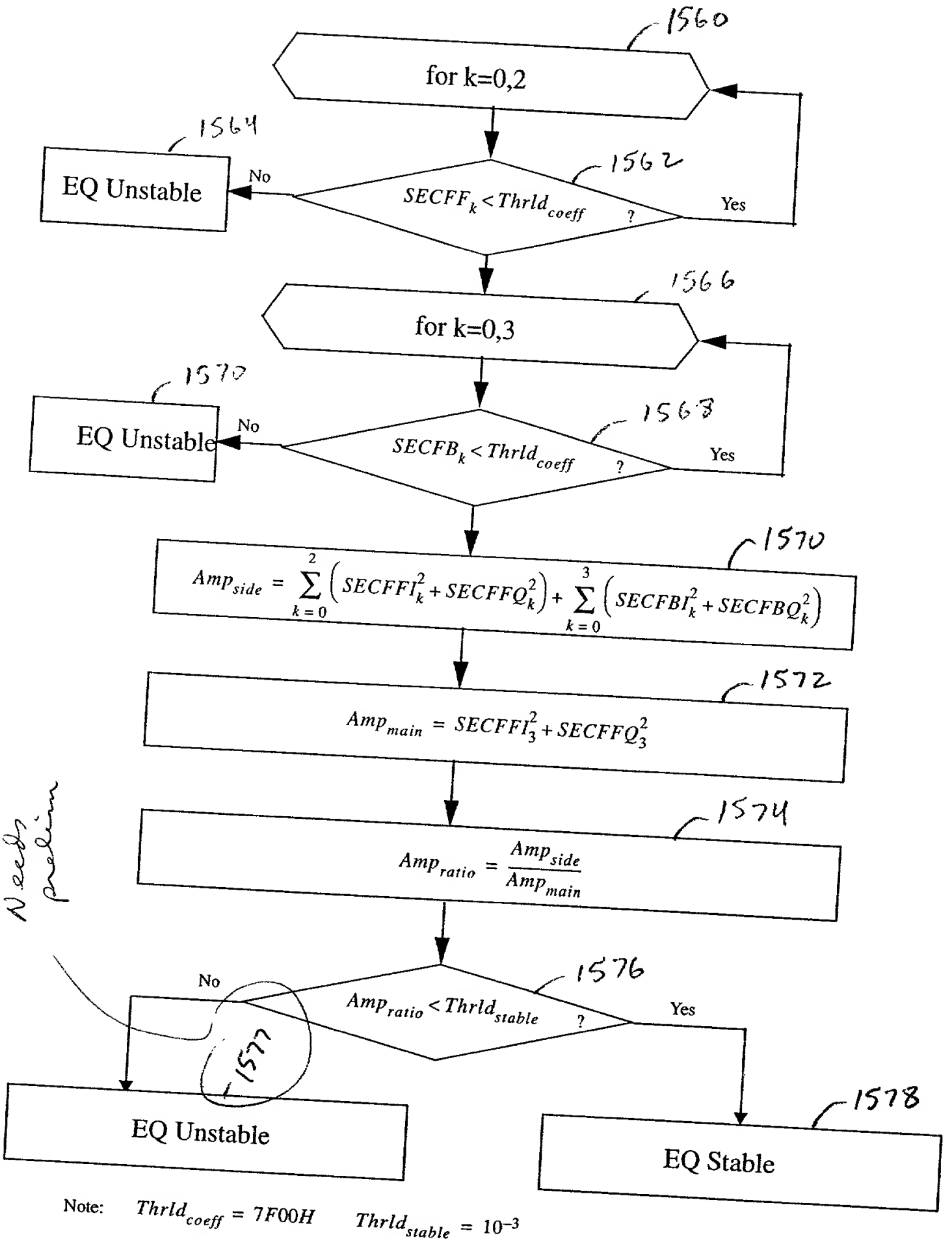
Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

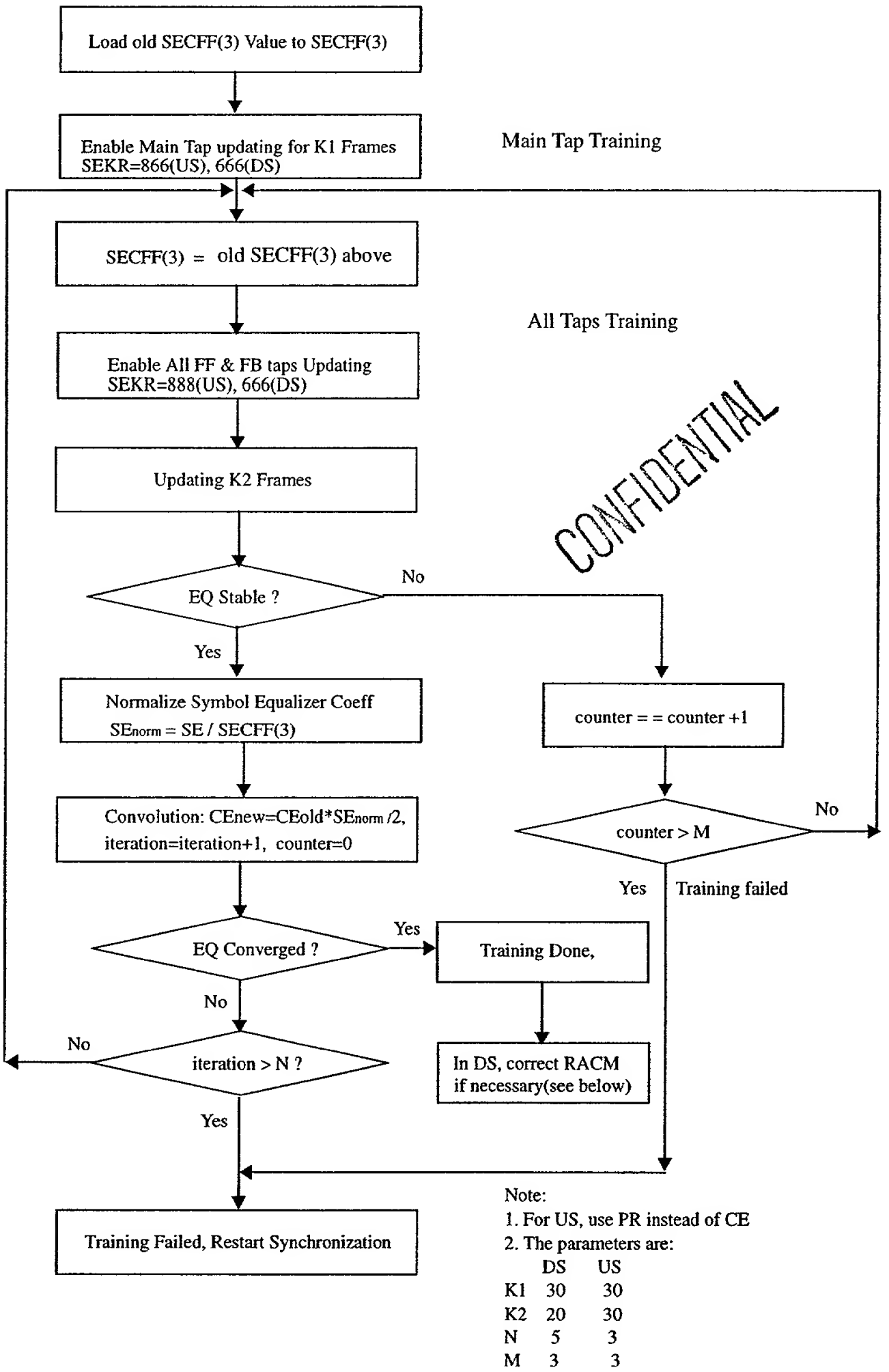
EQ Stability Check



Note: $Thrld_{coeff} = 7F00H$ $Thrld_{stable} = 10^{-3}$

FIG. 61

Periodic 2-Step Training Algorithm

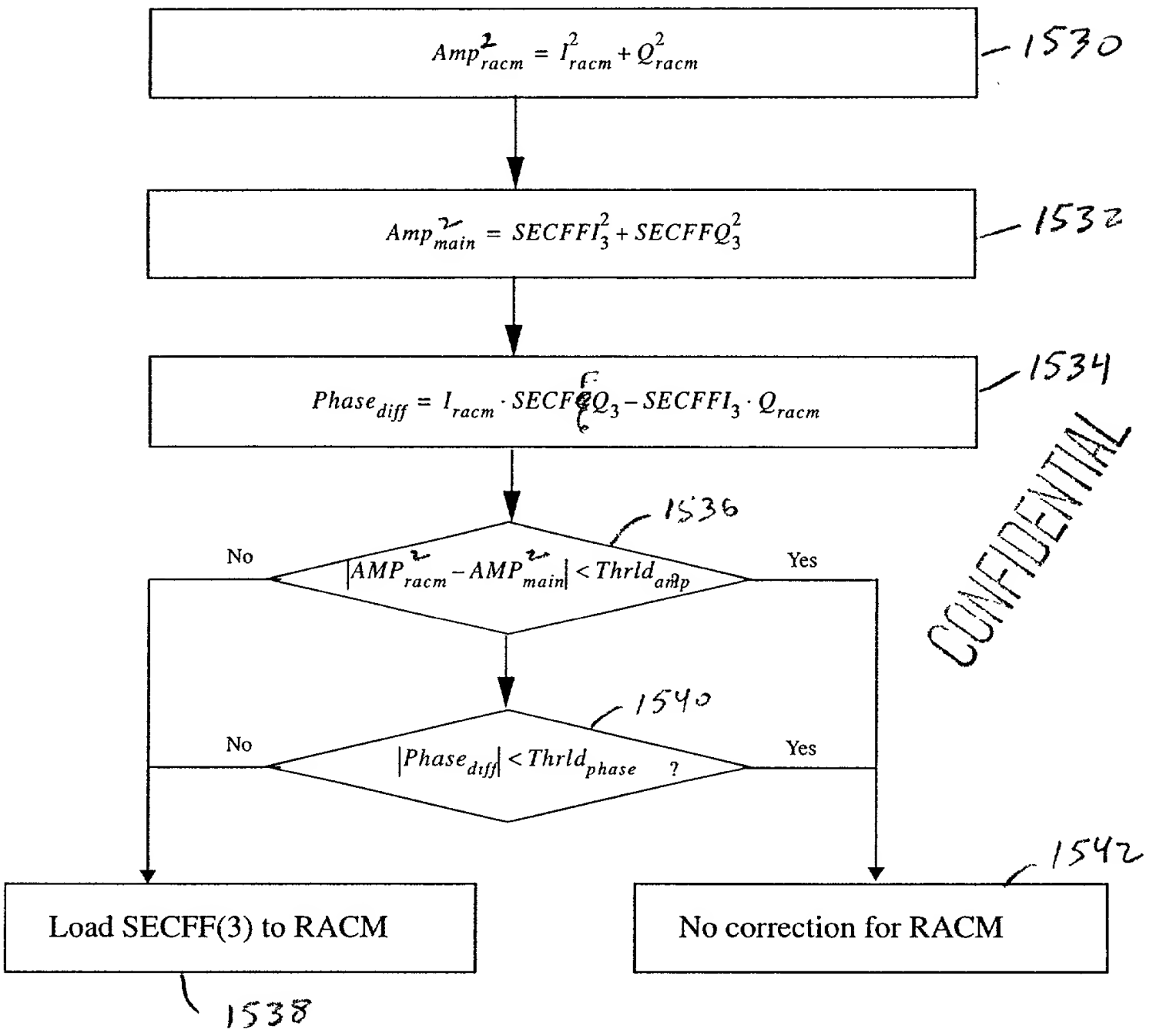


Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



Note: $Thrld_{amp} = TBD$

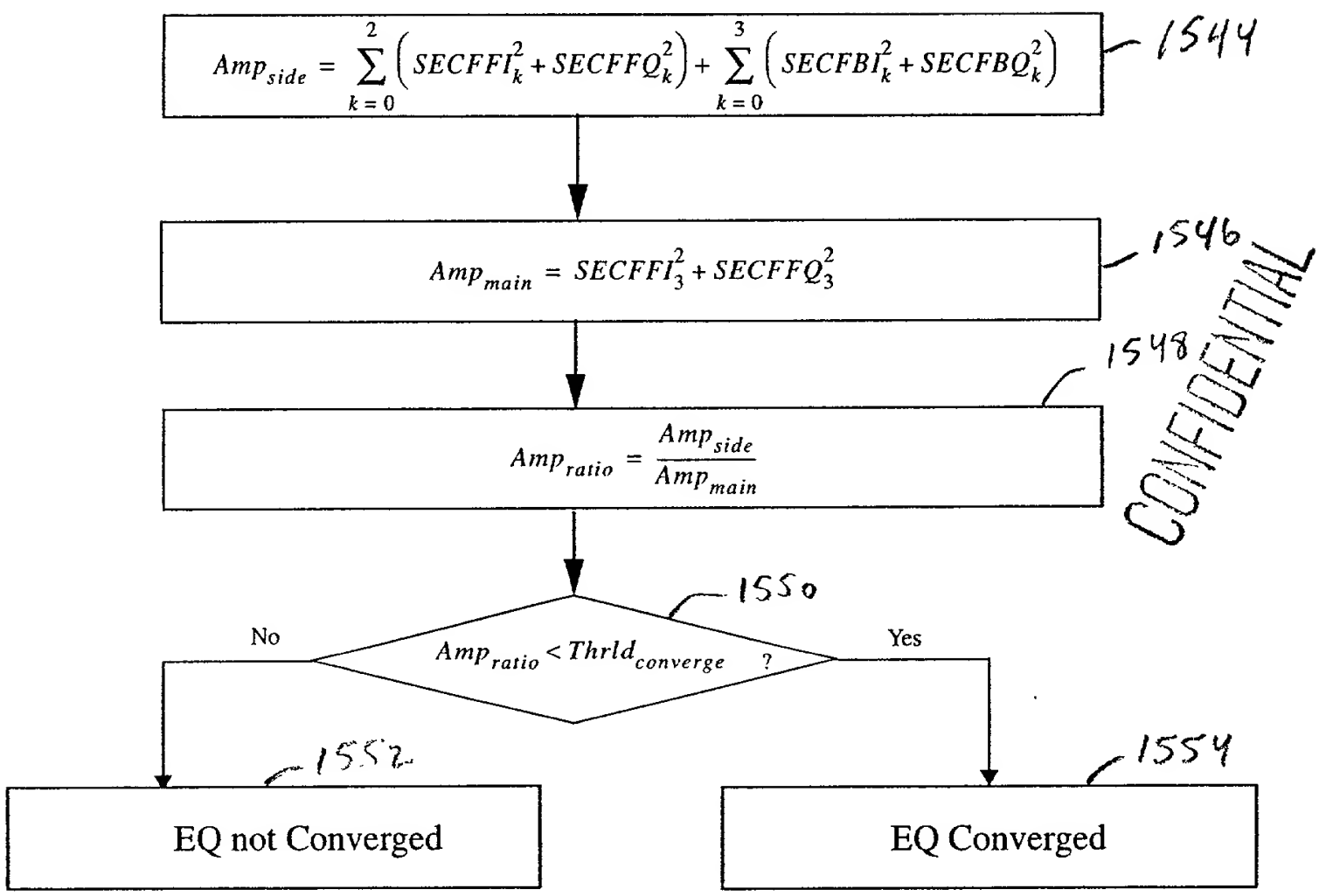
$Thrld_{phase} = TBD$

CONFIDENTIAL

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63.

EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart

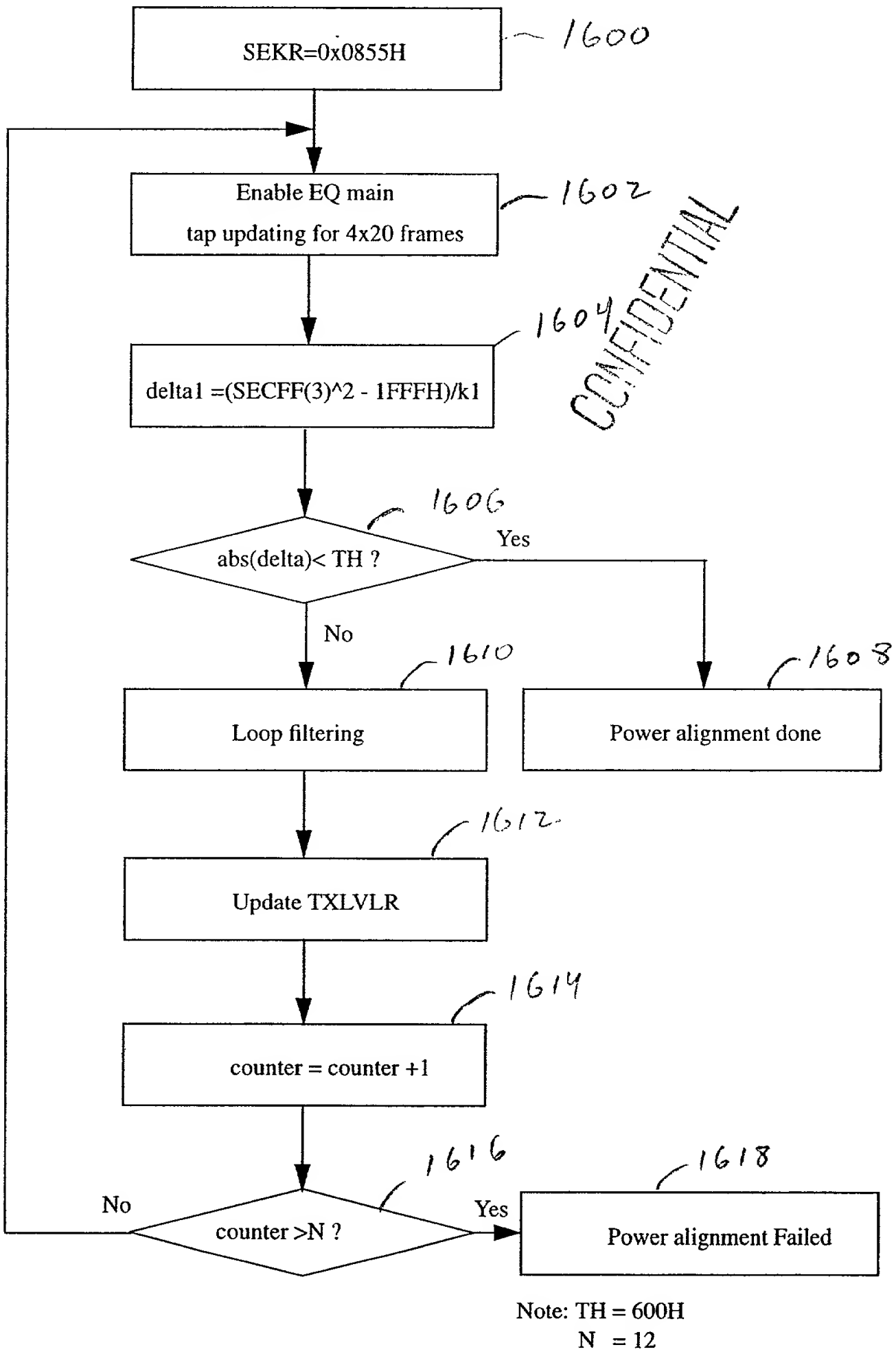


FIG. 65

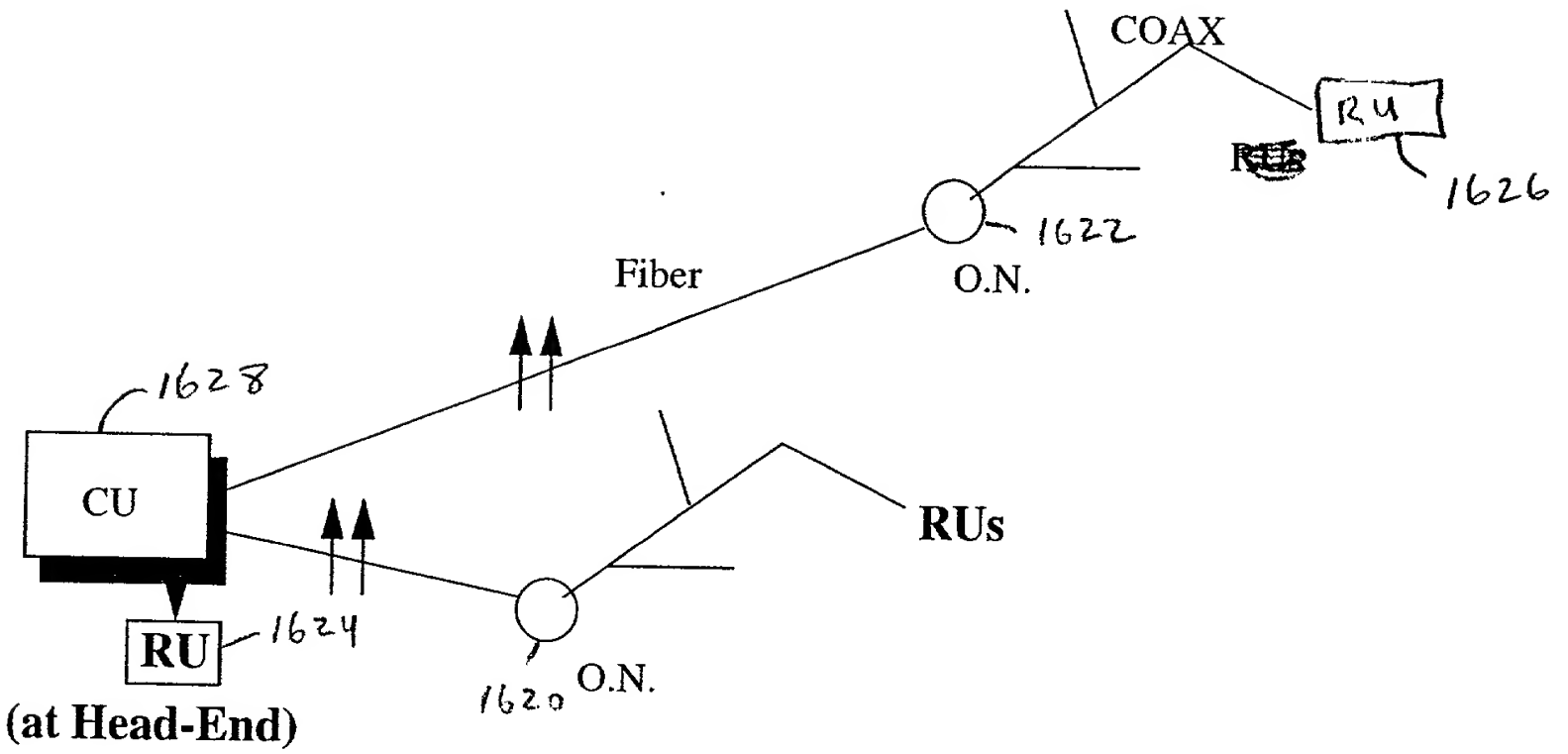
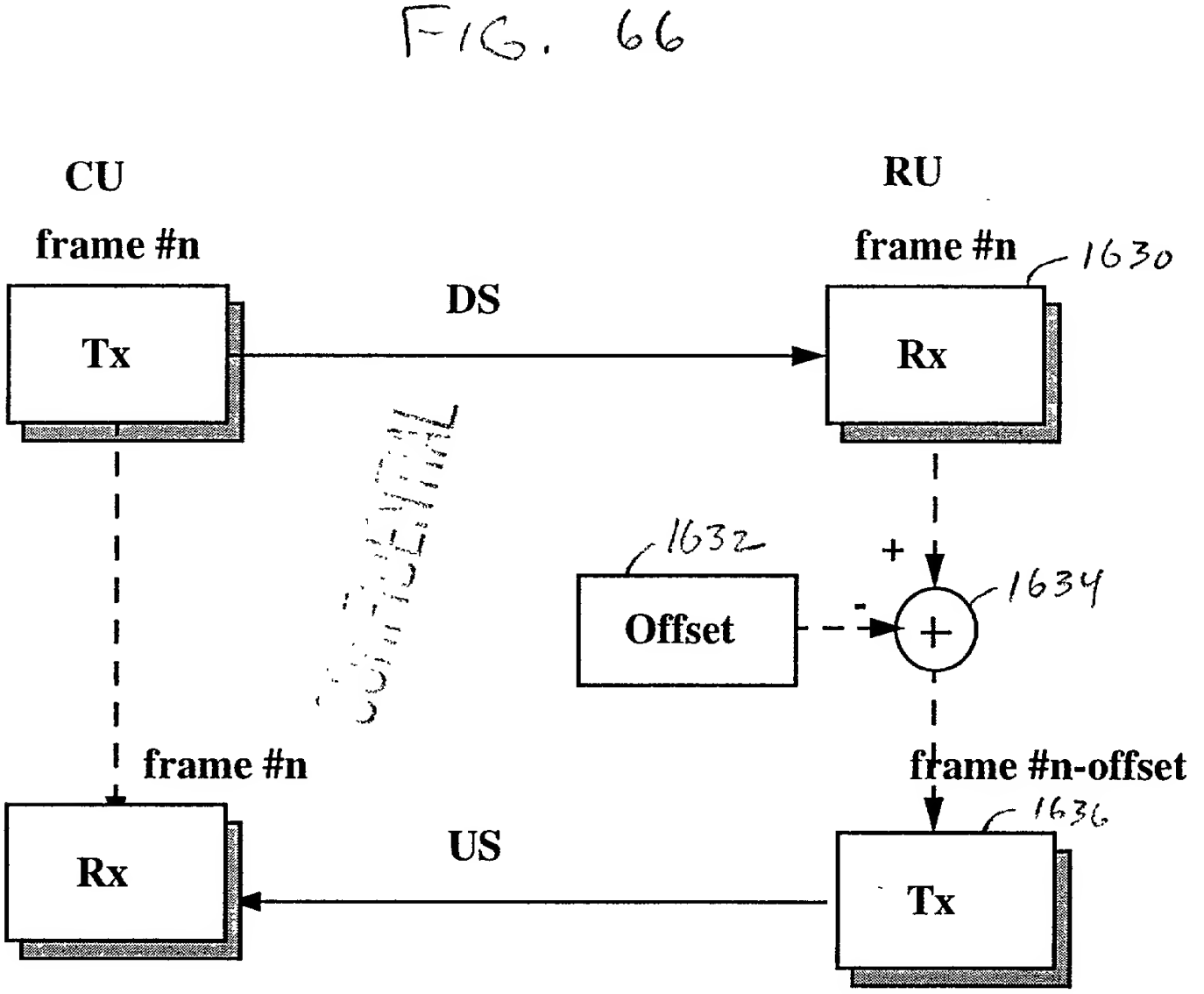


FIG. 66



Total Turn Around (TTA) in frames = Offset

FIG. 67

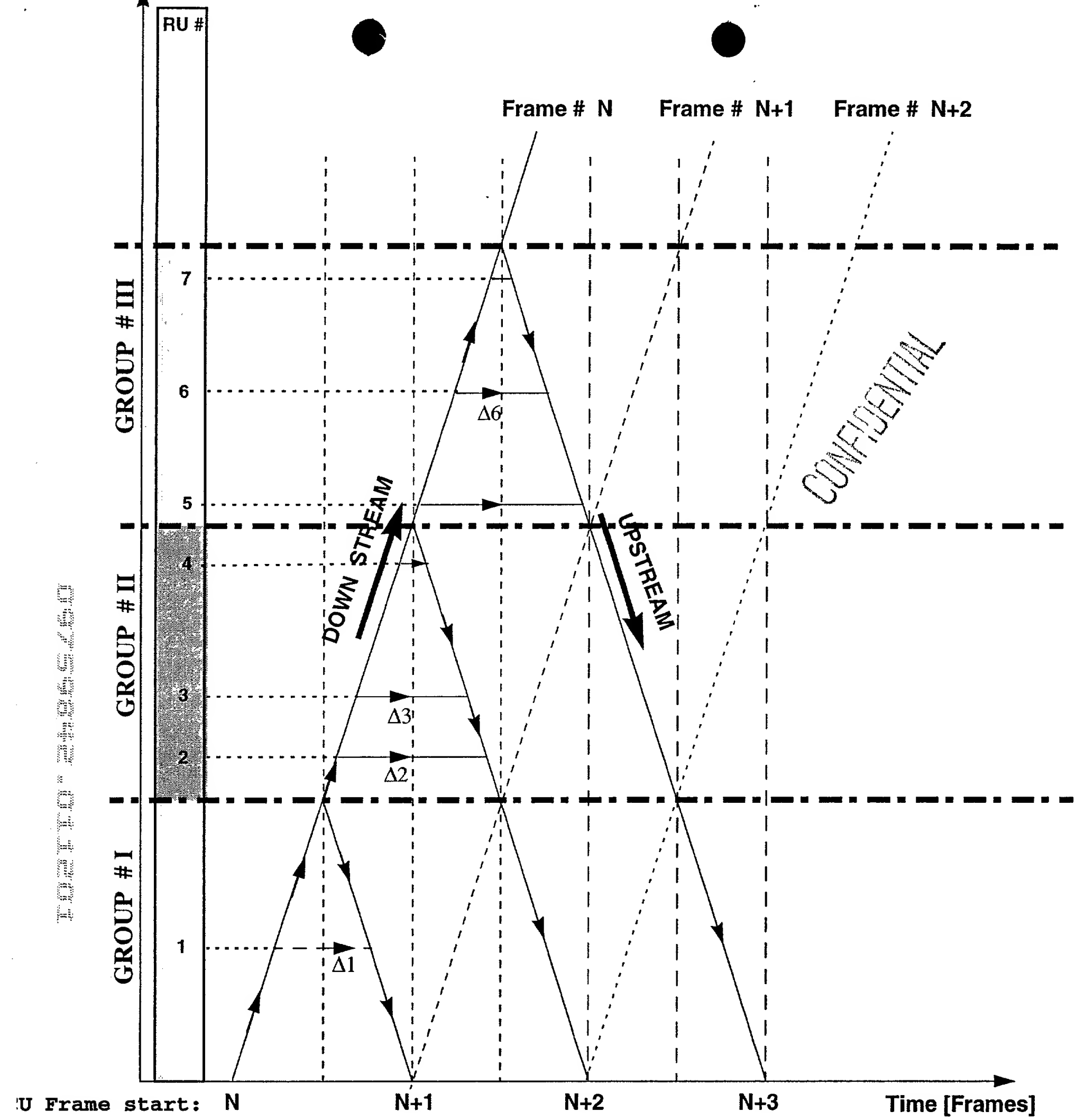


FIG. 68

~~Figure 3.1: Frame start propagation along the channel~~

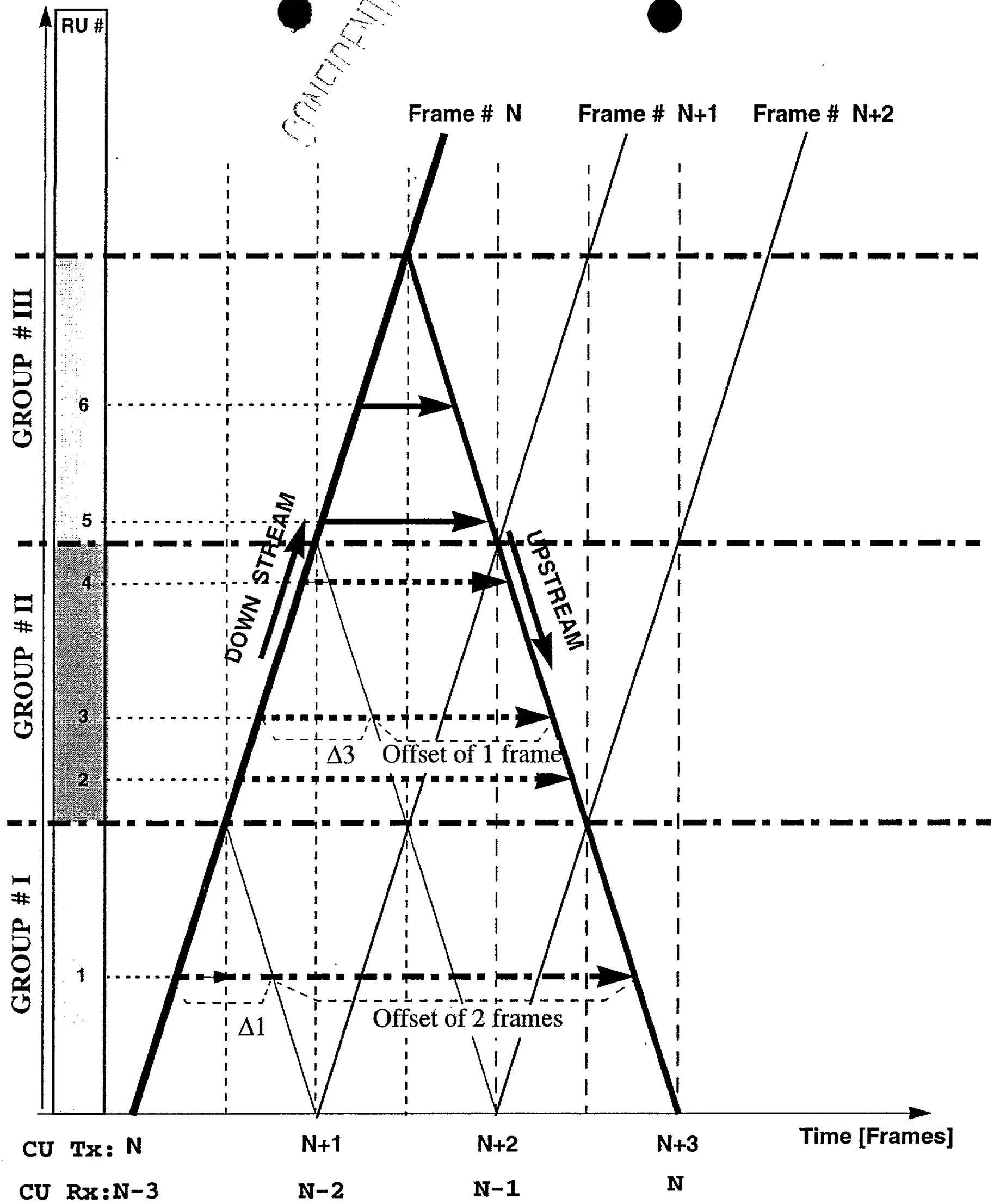


FIG. 69

Figure 69 Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

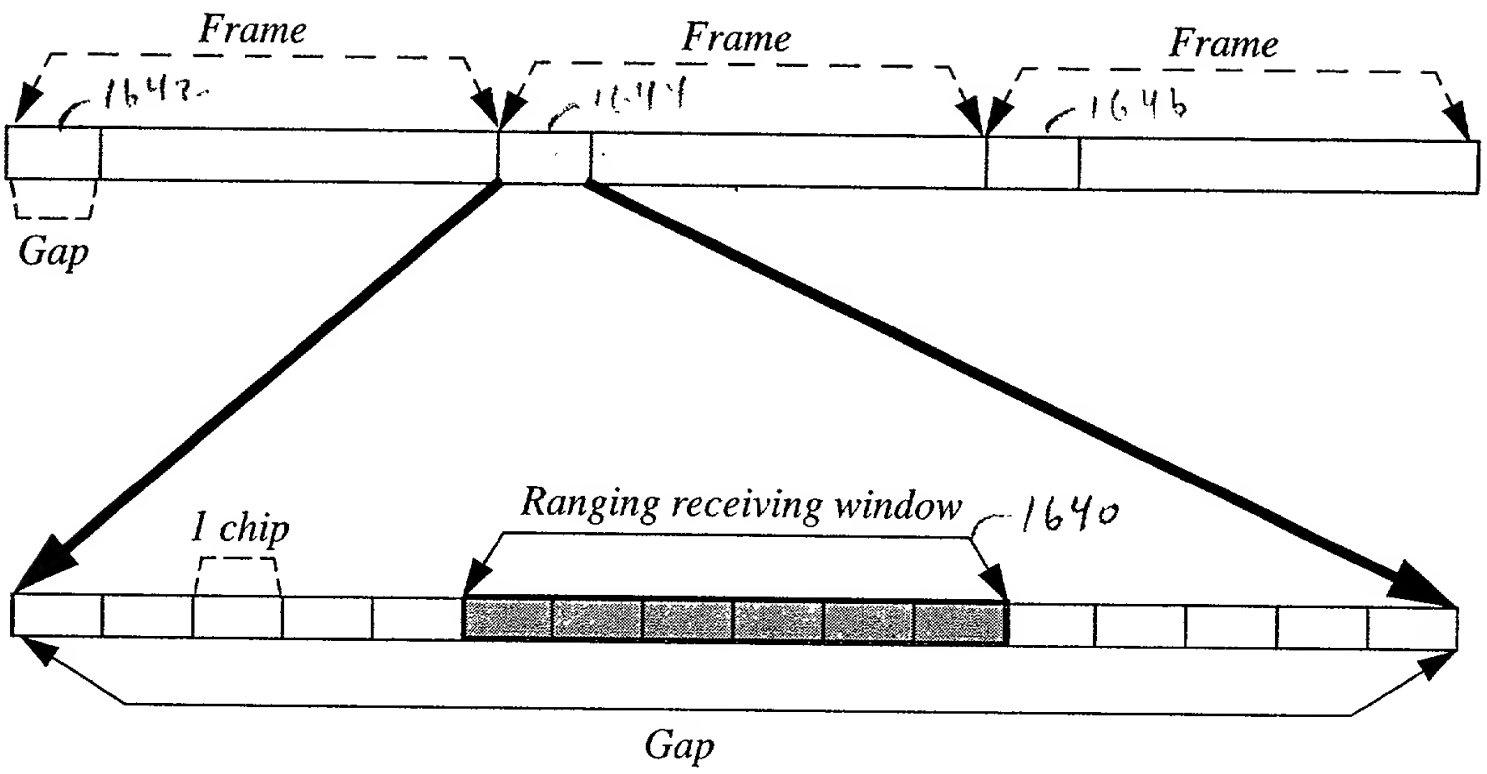

Frame
Frame
Frame
1642
1644
1646
Gap
1 chip
Ranging receiving window
1640
Gap

FIG. 7D

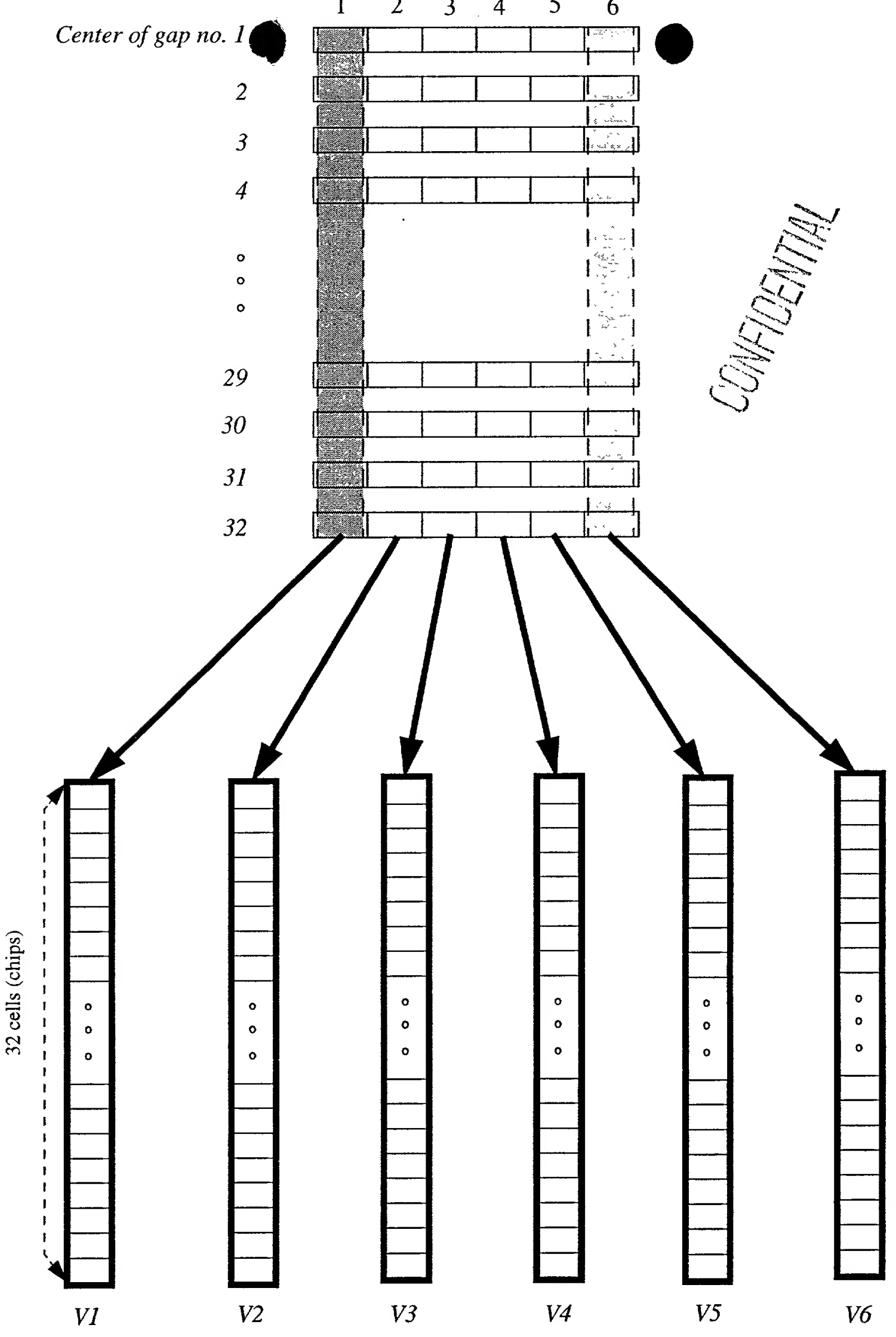


Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 7I

6

Chip\FR	1	2	3	4	5	6	7		33
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**...**	**0**
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72

UPSTREAM EQUALIZATION

CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.

1116

RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.

1118

CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.

1120

TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.

1122

AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.

IN CU

1124

CONVOLVE SE CIRCUIT WITH OLD COEFFICIENTS AND LOAD NEWLY CALCULATED COEFFICIENTS INTO RU XMTR PRECODE FILTER

RU

~~RU SENDS~~ FINAL FFE & DFE COEFFICIENTS ~~INTO~~ PRECODE FFE/DFE FILTER IN TRANSMITTER

TRANSPARENCY VALUES

1126

CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO ~~ONE~~ FOR RECEPTION OF UPSTREAM PAYLOAD DATA.

54B

FIG. ~~45B~~

53B

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FROM FIG. 45B

DOWNSTREAM EQUALIZATION

1128

CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

1130

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

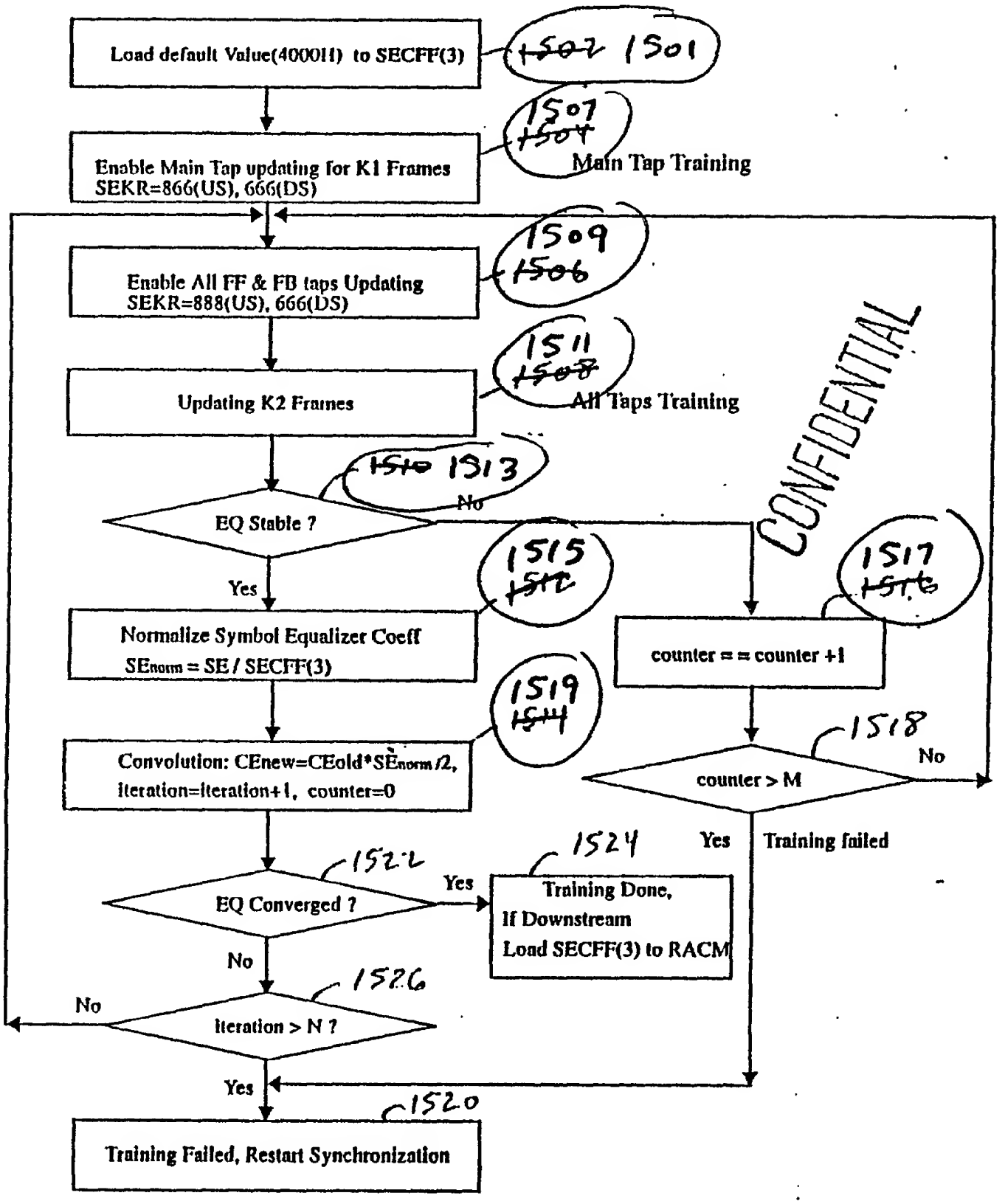
1132

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND ~~LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764~~; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AND DFE FILTERS OF CE CIRCUIT 764 AND LOADS THE NEWLY CALCULATED TAP WEIGHTS INTO THE FFE AND DFE FILTERS OF THE CE CIRCUIT

~~54C~~
FIG. ~~45C~~
53C

Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60